

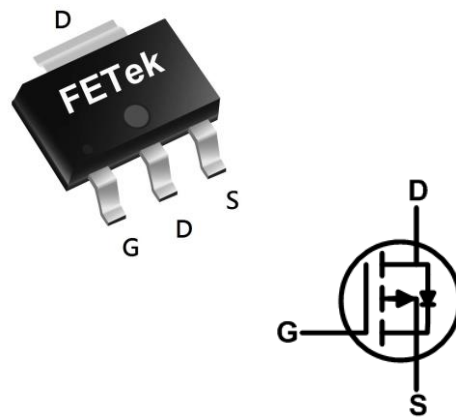
- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

**Product Summary**


BVDSS	RDSON	ID
-60V	180mΩ	-2.3A

**Description**

The FKL6107 is the high cell density trenched P-ch MOSFETs, which provides excellent RDSON and efficiency for most of the small power switching and load switch applications. The FKL6107 meets the RoHS and Green Product requirement with full function reliability approved.

**SOT223 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-2.3	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-1.8	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-12	A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>3</sup>	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	48	$^\circ C/W$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.038	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-2A$	---	140	180	$\text{m}\Omega$
		$V_{GS}=-5V, I_D=-1.5A$	---	200	260	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.5	-2.0	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.92	---	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=-48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$	---	5.3	---	S
$Q_g$	Total Gate Charge (-10V)	$V_{DS}=-48V, V_{GS}=-10V, I_D=-2A$	---	8.3	11.6	nC
$Q_{gs}$	Gate-Source Charge		---	1.8	2.52	
$Q_{gd}$	Gate-Drain Charge		---	1.6	2.25	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=-30V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-2A$	---	4.1	8.2	ns
$T_r$	Rise Time		---	21	38	
$T_{d(off)}$	Turn-Off Delay Time		---	20.3	40.6	
$T_f$	Fall Time		---	21	42	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	428	600	pF
$C_{oss}$	Output Capacitance		---	39	55	
$C_{rss}$	Reverse Transfer Capacitance		---	26	36.4	

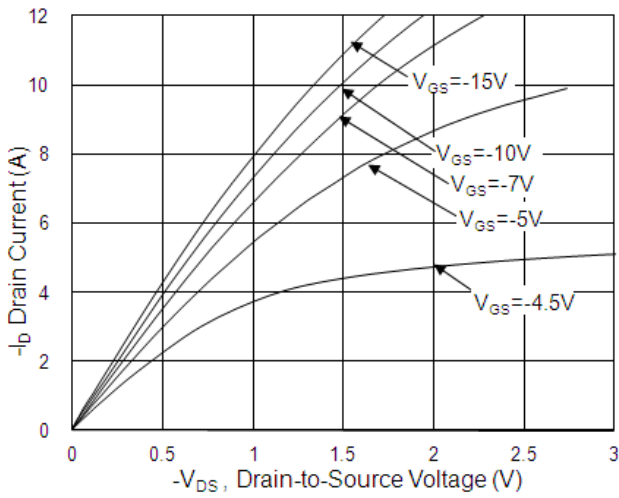
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	-2.3	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	-12	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

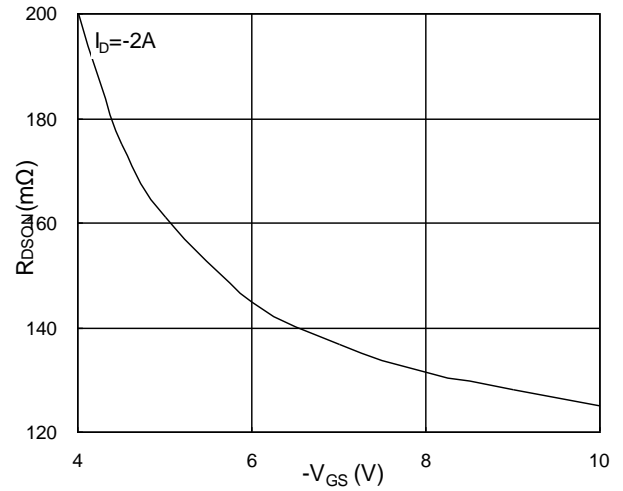
## Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

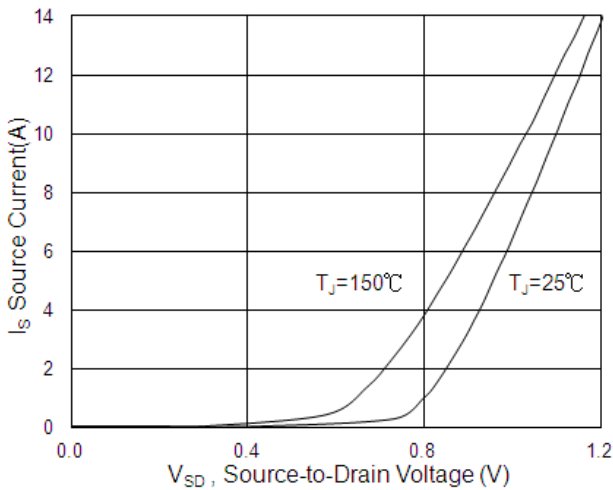
**Typical Characteristics**



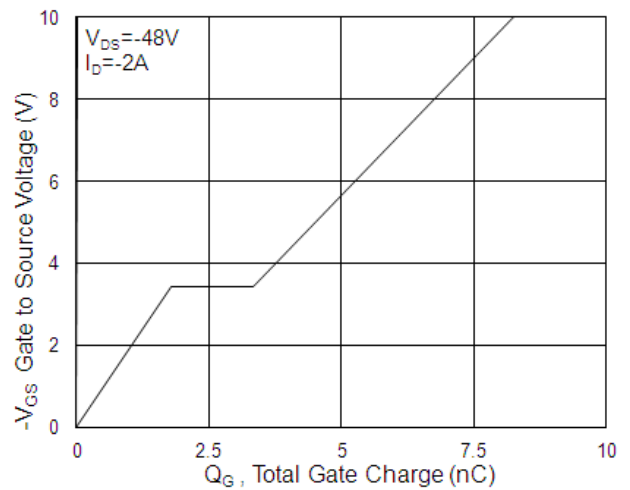
**Fig.1 Typical Output Characteristics**



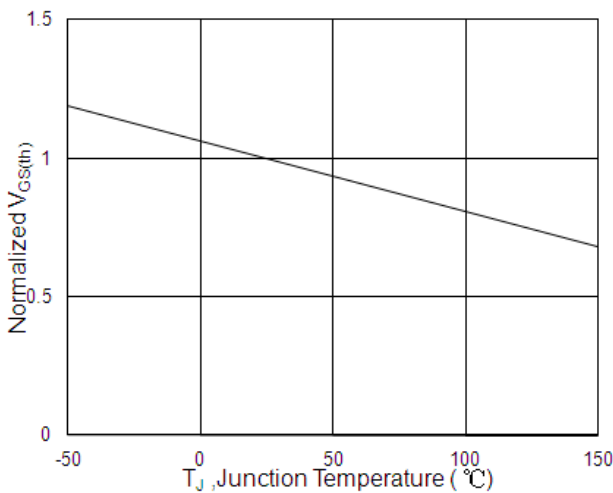
**Fig.2 On-Resistance vs. Gate-Source Voltage**



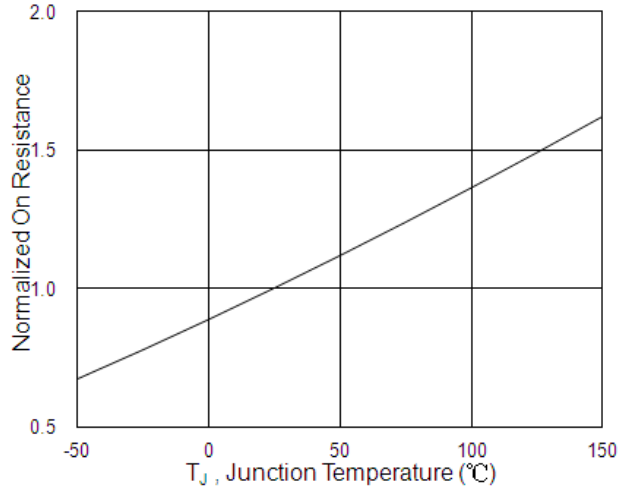
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

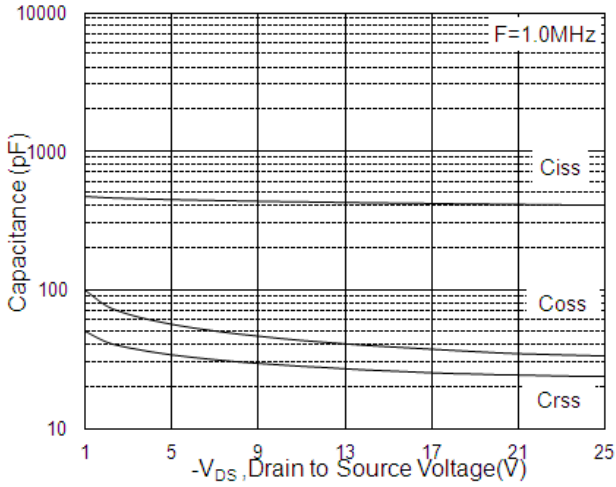


Fig.7 Capacitance

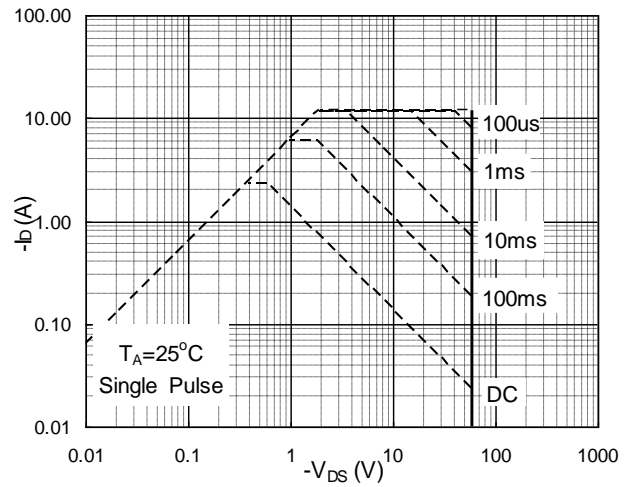


Fig.8 Safe Operating Area

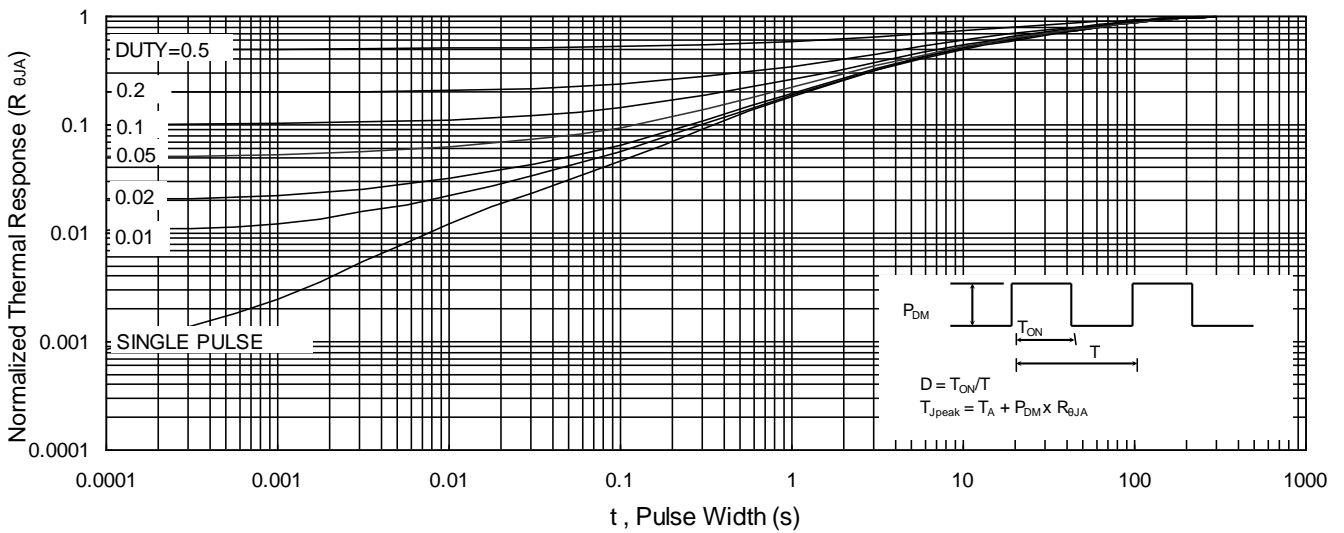


Fig.9 Normalized Maximum Transient Thermal Impedance

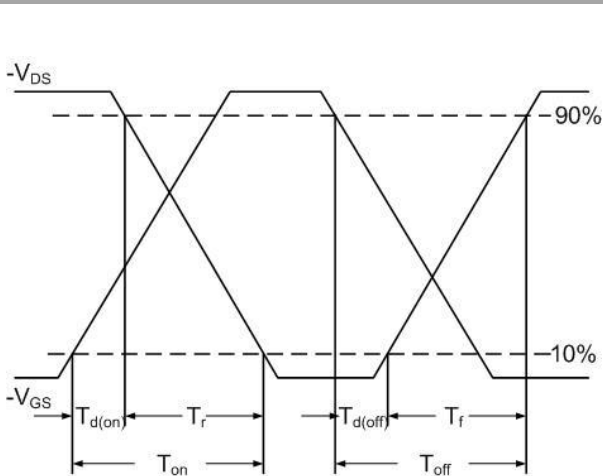


Fig.10 Switching time waveform

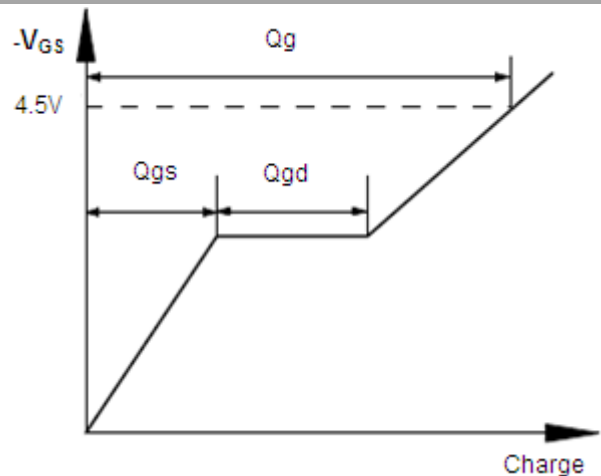


Fig.11 Gate Charge waveform