

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

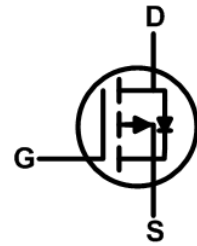
**Product Summary**


BVDSS	RDSON	ID
-60V	35mΩ	-29A

**Description**

The FKD6105 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKD6105 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

**TO252 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-29	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-18.5	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-6.2	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-5.0	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-58	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	64.8	mJ
$I_{AS}$	Avalanche Current	-36	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	45	W
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	2	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	2.8	$^\circ C/W$

Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-10V, I_D=-20A$	---	30	35	m $\Omega$
		$V_{GS}=-4.5V, I_D=-15A$	---	38	55	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	-1.6	-2.5	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	$\mu A$
		$V_{DS}=-48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-20A$	---	30	---	S
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-15A$	---	24	---	nC
$Q_{gs}$	Gate-Source Charge		---	8.6	---	
$Q_{gd}$	Gate-Drain Charge		---	7.3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-15A$	---	9	---	ns
$T_r$	Rise Time		---	70.7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	59.8	---	
$T_f$	Fall Time		---	20.4	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	2217	---	pF
$C_{oss}$	Output Capacitance		---	310	---	
$C_{rss}$	Reverse Transfer Capacitance		---	238	---	

## Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	-29	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V
$t_{rr}$	Reverse Recovery Time	$I_F=-20A, di/dt=100A/\mu s$ ,	---	30	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	45	---	nC

Note :

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- The EAS data shows Max. rating. The test condition is  $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-36A$
- The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

Typical Characteristics

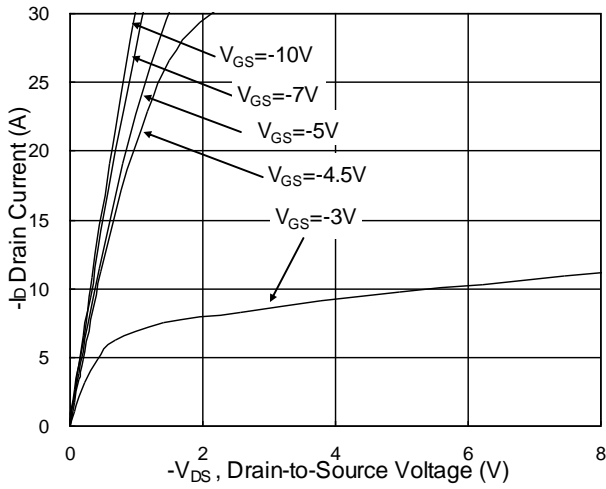


Fig.1 Typical Output Characteristics

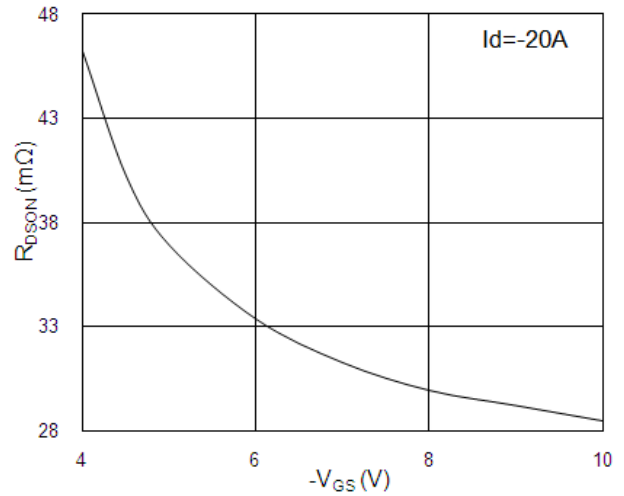


Fig.2 On-Resistance vs G-S Voltage

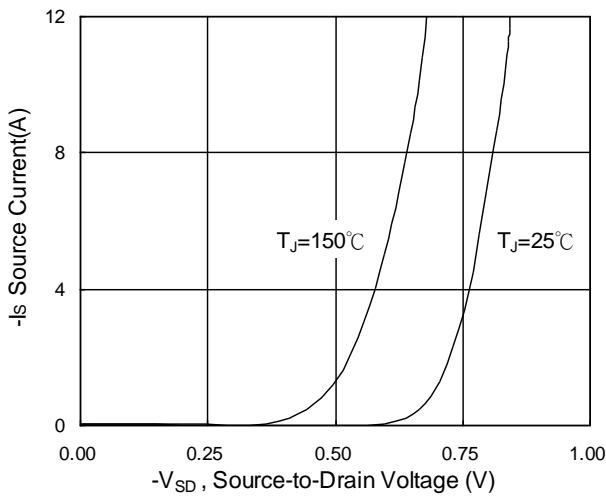


Fig.3 Source Drain Forward Characteristics

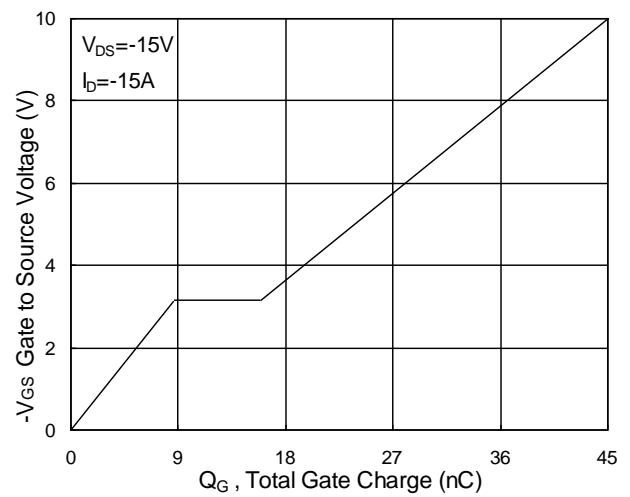


Fig.4 Gate-charge Characteristics

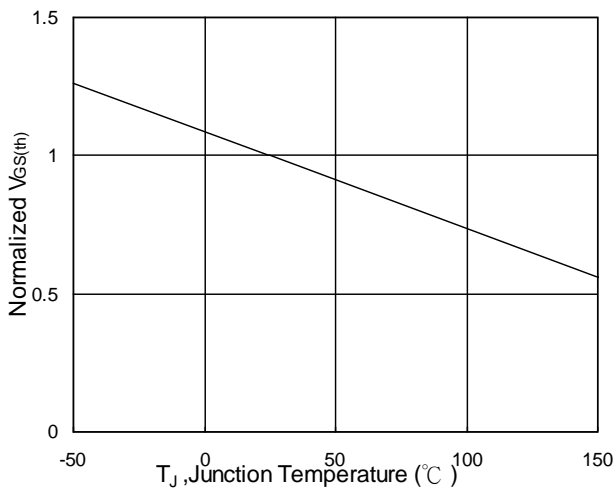


Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$

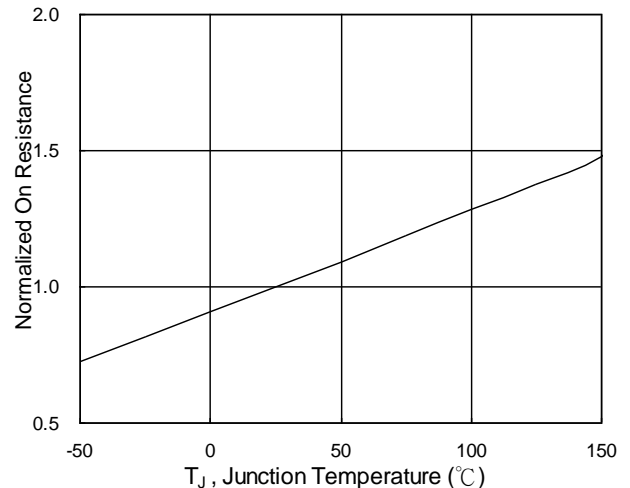


Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$

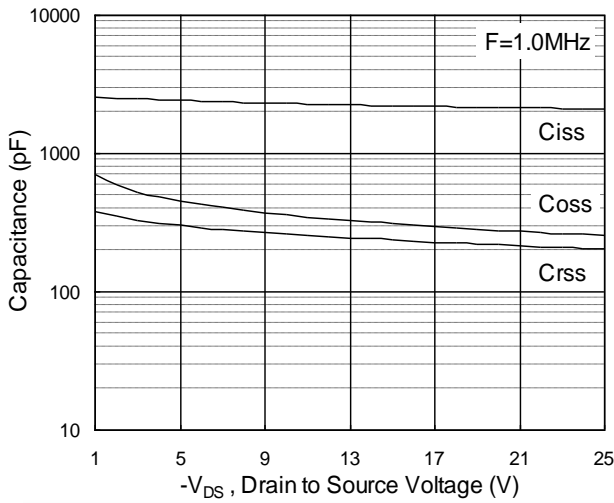


Fig.7 Capacitance

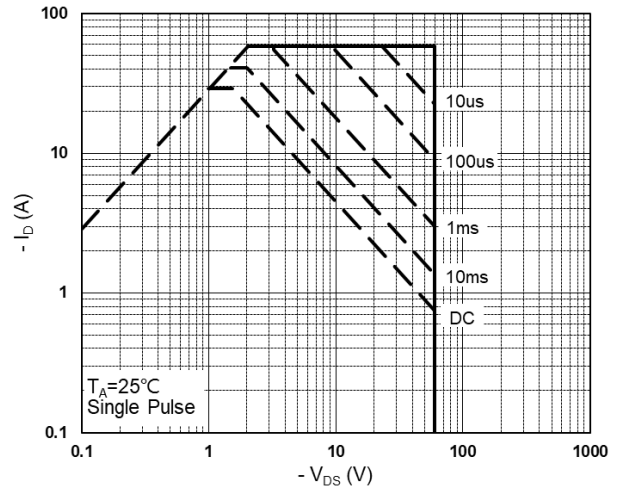


Fig.8 Safe Operating Area

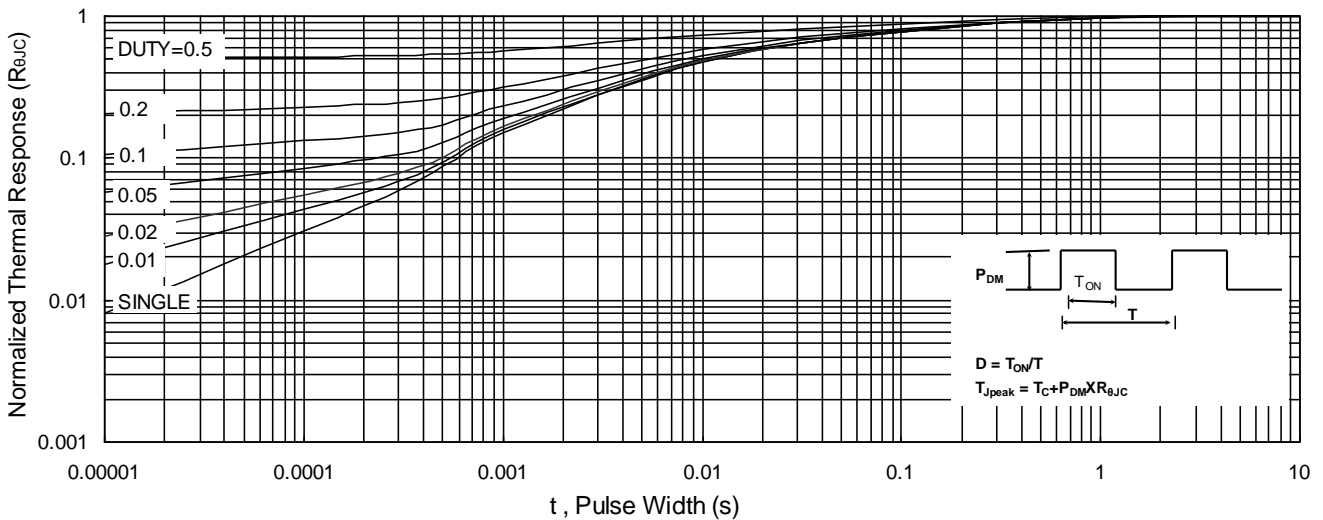


Fig.9 Normalized Maximum Transient Thermal Impedance

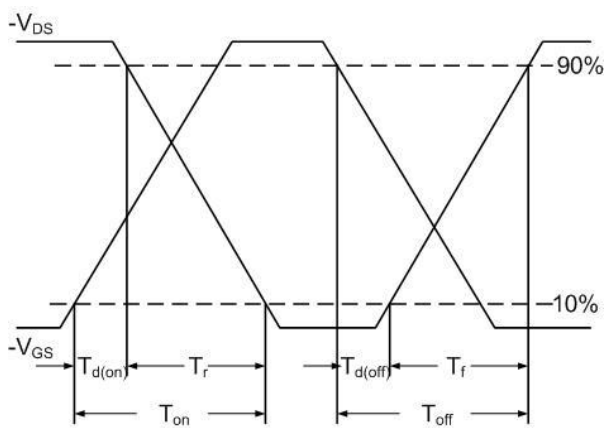


Fig.10 Switching Time Waveform

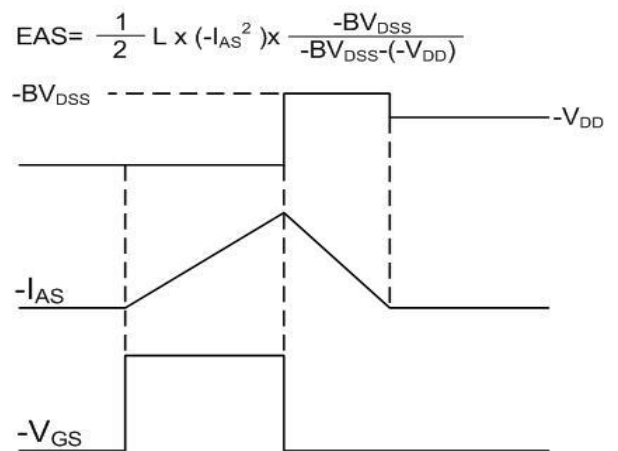


Fig.11 Unclamped Inductive Waveform