FKD6101

P-Ch 60V Fast Switching MOSFETs

★ Super Low Gate Charge
★ 100% EAS Guaranteed
★ Green Device Available
★ Excellent CdV/dt effect decline
★ Advanced high cell density Trench technology

Product Summery

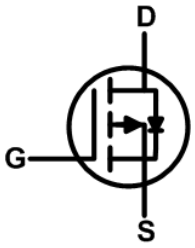
BVDSS	RDSON	ID
-60V	140mΩ	-9.5A

Description

The FKD6101 is the high cell density trenched P-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKD6101 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

TO252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-60	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25°C	Continuous Drain Current, V_{GS} @ -10V[1]	-12	A
I_D@T_C=100°C	Continuous Drain Current, V_{GS} @ -10V[1]	-7.8	A
I_D@T_A=25°C	Continuous Drain Current, V_{GS} @ -10V[1]	-3.5	A
I_D@T_A=70°C	Continuous Drain Current, V_{GS} @ -10V[1]	-2.8	A
I_{DM}	Pulsed Drain Current[2]	-25	A
EAS	Single Pulse Avalanche Energy[3]	20	mJ
I_{AS}	Avalanche Current	-20	A
P_D@T_C=25°C	Total Power Dissipation[4]	25	W
P_D@T_A=25°C	Total Power Dissipation[4]	2	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	62	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	5	°C/W

Electrical Characteristics (T_J=25 ˚C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-60	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25˚C , I_D=-1mA	---	-0.049	---	V/˚C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-8A	---	---	140	mΩ
		V_{GS}=-4.5V , I_D=-6A	---	---	190	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	---	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	5.42	---	mV/˚C
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-48V , V_{GS}=0V , T_J=25˚C	---	---	1	uA
		V_{DS}=-48V , V_{GS}=0V , T_J=150˚C	---	---	5	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-5A	---	5.8	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-20V , V_{GS} =-4.5V , I_D=-5A	---	5.85	---	nC
Q_{gs}	Gate-Source Charge		---	2.9	---	
Q_{gd}	Gate-Drain Charge		---	1.8	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-12V , V_{GS}=-10V , R_G=3.3Ω, I_D=-5A	---	10	---	ns
T_r	Rise Time		---	17	---	
$T_{d(off)}$	Turn-Off Delay Time		---	22	---	
T_f	Fall Time		---	21	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , F=1MHz	---	715	---	pF
C_{oss}	Output Capacitance		---	51	---	
C_{rss}	Reverse Transfer Capacitance		---	34	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-9.5	A
I_{SM}	Pulsed Source Current[2,5]		---	---	-24	A
V_{SD}	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25˚C	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	I_F=-8A , dI/dt=100A/μs , T_J=25˚C	---	10.2	---	nS
Q_{rr}	Reverse Recovery Charge		---	5.4	---	nC

Note :
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3. The EAS data shows Max. rating. The test condition is V_{DD}=-25V,V_{GS}=-10V,L=0.1mH,I_{AS}=-15A
4. The power dissipation is limited by 150˚C junction temperature
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

P-Channel Typical Characteristics

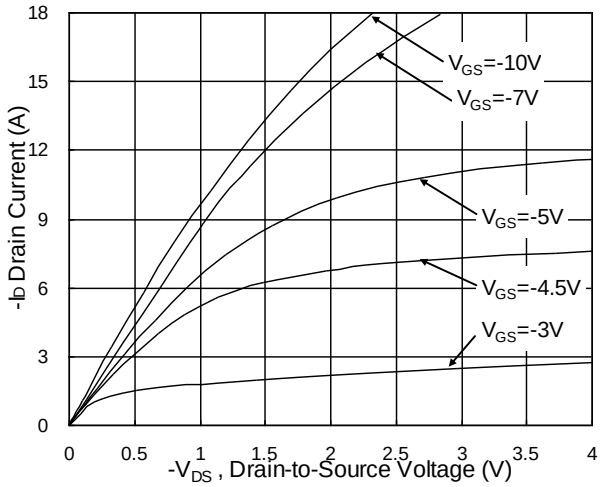


Fig.1 Typical Output Characteristics

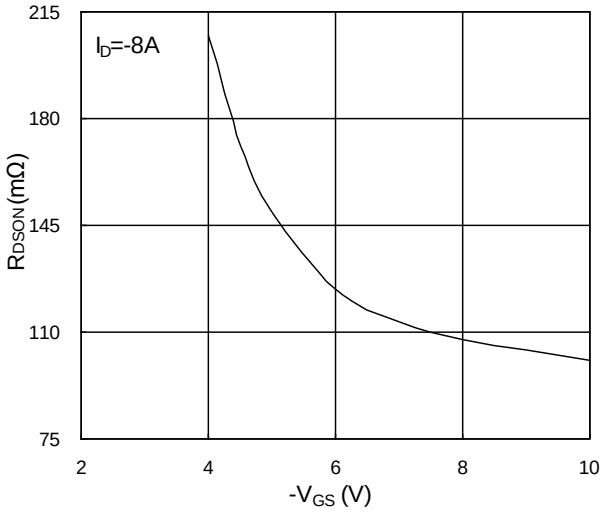


Fig.2 On-Resistance vs. G-S Voltage

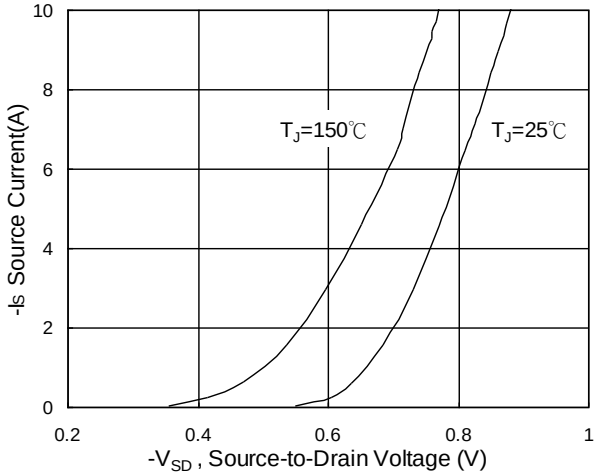


Fig.3 Forward Characteristics Of Reverse

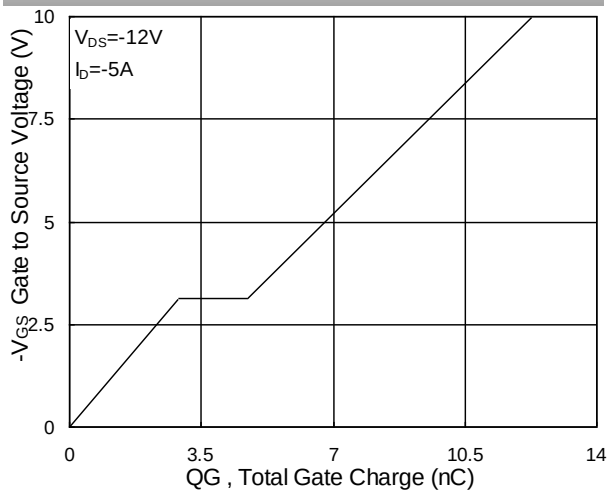


Fig.4 Gate-Charge Characteristics

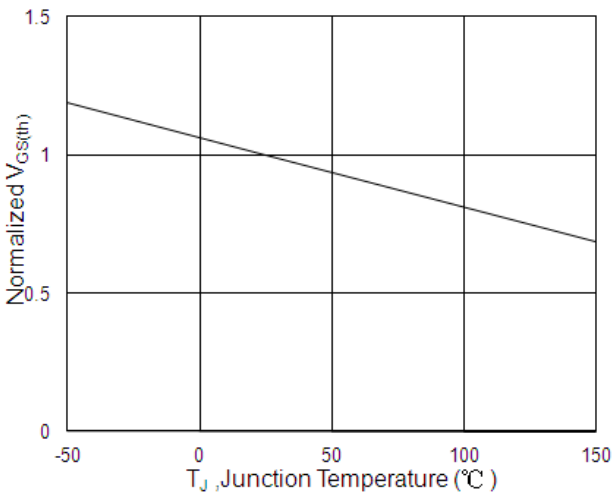


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

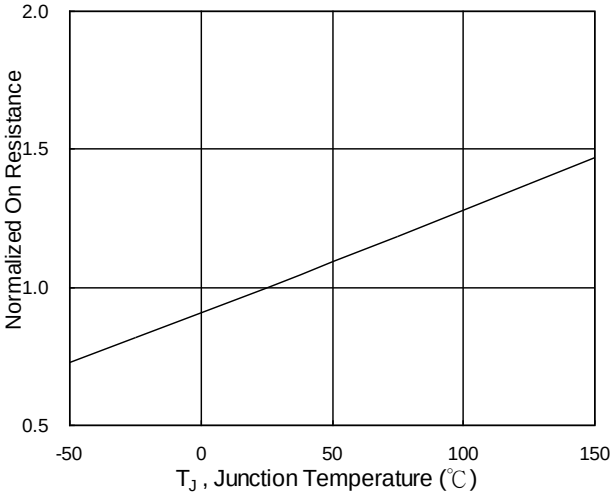


Fig.6 Normalized R_{DSON} vs. T_J

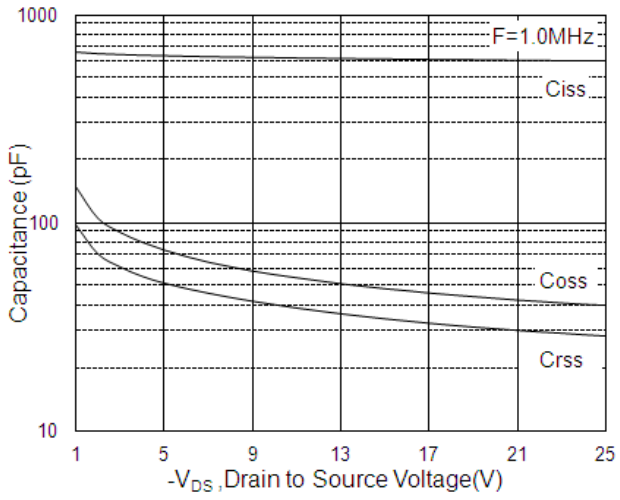


Fig.7 Capacitance

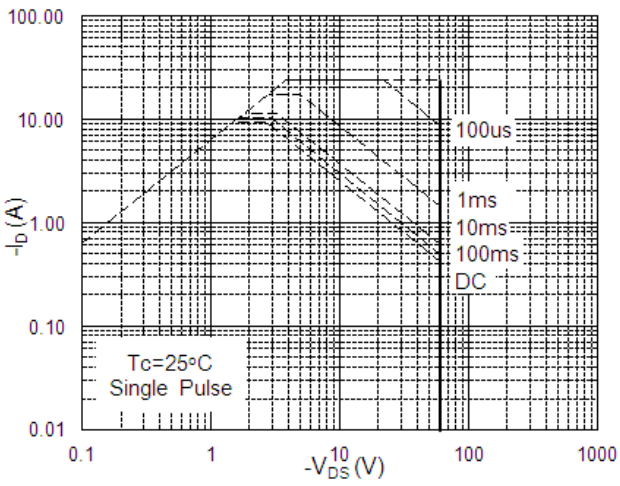


Fig.8 Safe Operating Area

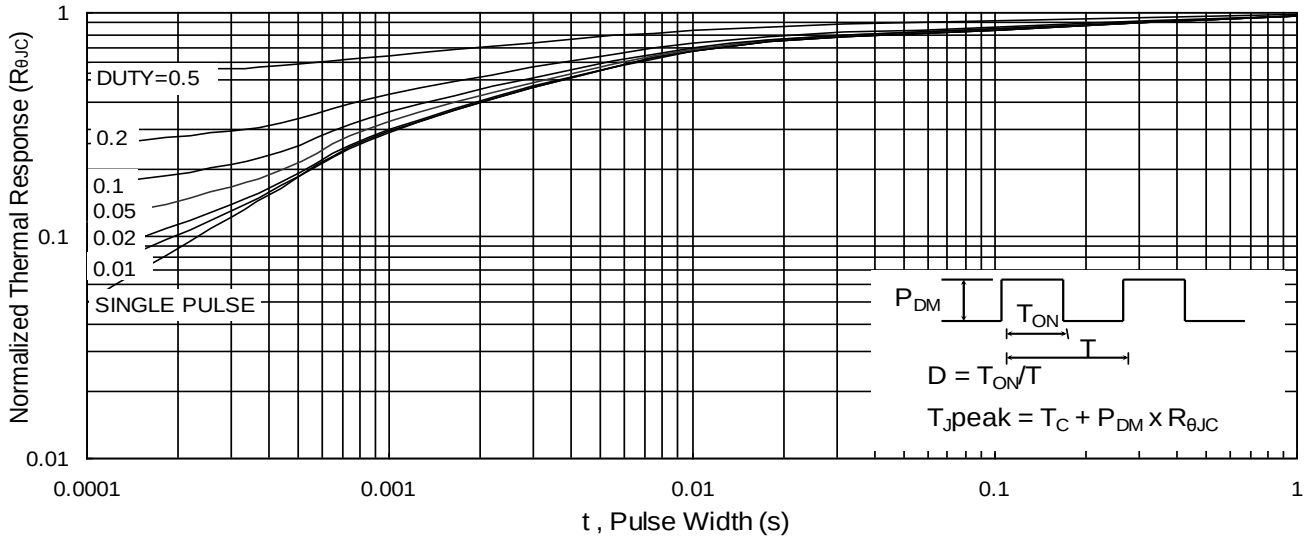


Fig.9 Normalized Maximum Transient Thermal Impedance

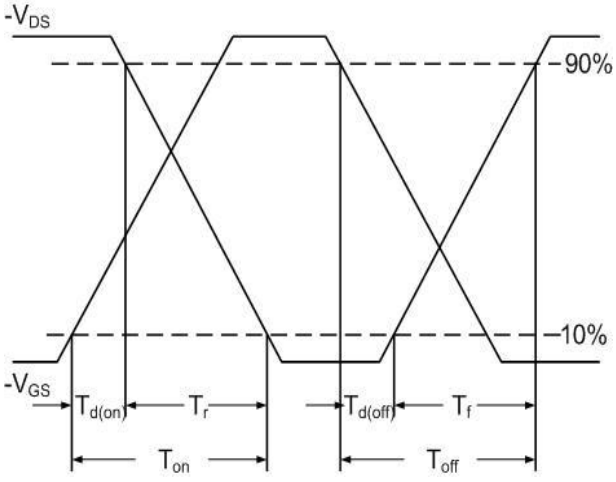


Fig.10 Switching Time Waveform

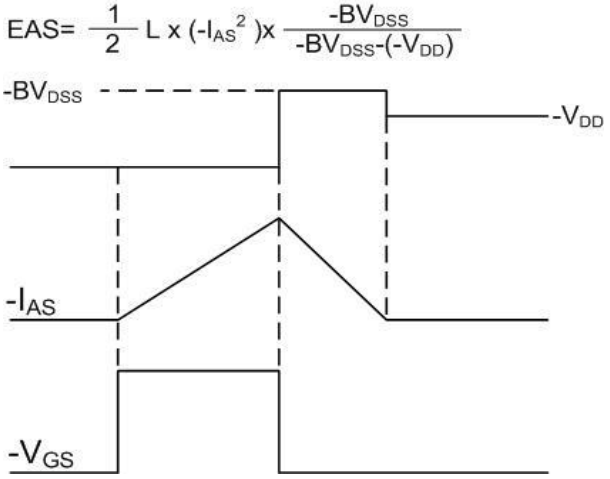


Fig.11 Unclamped Inductive Switching Waveform