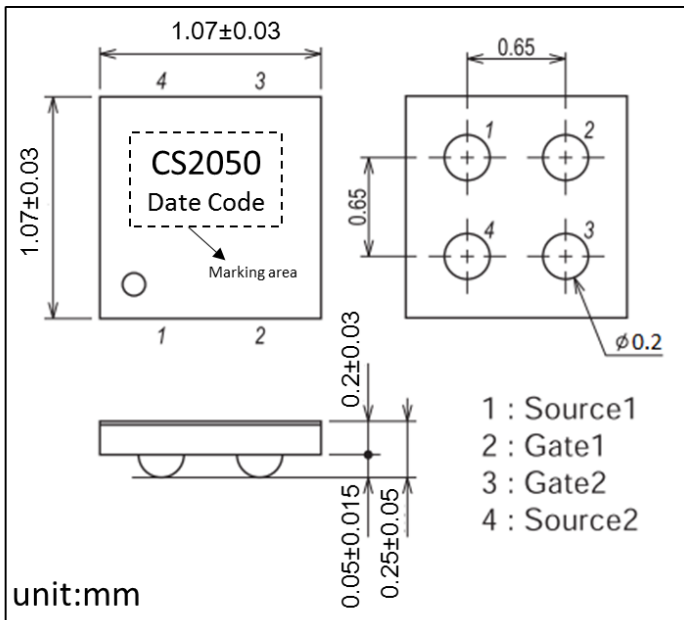
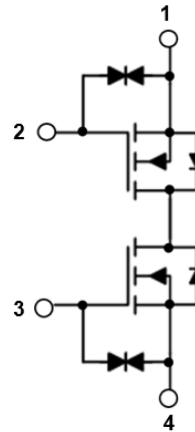
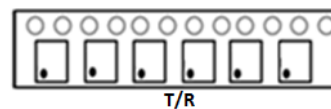



Features

- ★ 2.5V Drive
- ★ Common-drain type
- ★ ESD Protection

Product Summary

V _{SS}	R _{SS(ON)} Max	I _S Max
20V	36.0mΩ @ 4.5V	6A
	38.0mΩ @ 4.0V	
	48.0mΩ @ 3.1V	
	55.0mΩ @ 2.5V	

WLCSP Package Dimensions

Electrical Connection

Taping Type: T/R

Absolute Maximum Ratings (T_A=25°C)

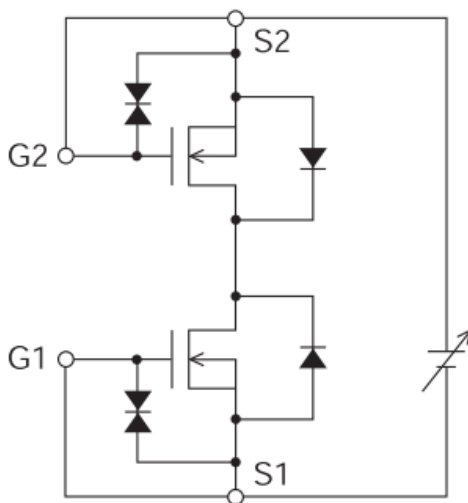
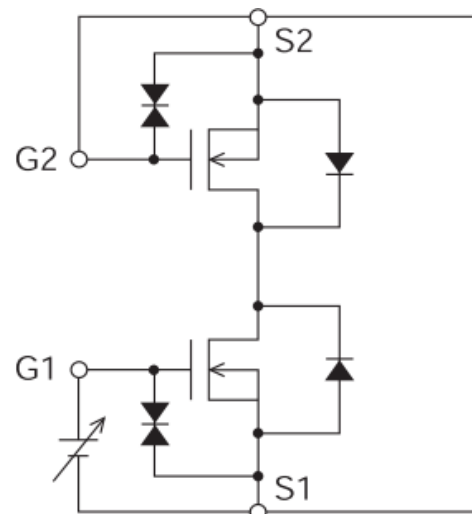
Symbol	Parameter	Rating	Units
V _{SS}	Source to Source Voltage	20	V
V _{GSS}	Gate to Source Voltage	±12	V
I _S	Continuous Source Current ¹	6	A
I _{SP}	Pulsed Source Current ²	60	A
P _T	Total Power Dissipation ¹	1.6	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Electrical Characteristics at $T_A=25^\circ\text{C}$

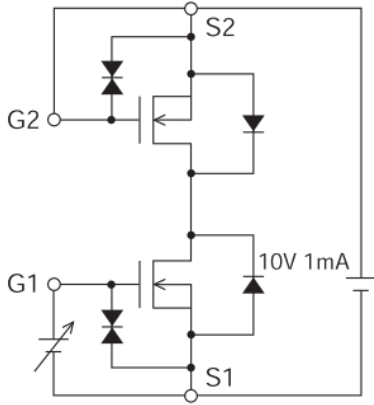
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{SSS}	Source-Source Breakdown Voltage	$V_{GS}=0V, I_S=250\mu A$	20	---	---	V
$R_{SS(ON)}$	Static Source-Source On-State Resistance	$V_{GS}=4.5V, I_S=1.5A$	23	32	36	m Ω
		$V_{GS}=4.0V, I_S=1.5A$	25	33	38	
		$V_{GS}=3.7V, I_S=1.5A$	26	34	41	
		$V_{GS}=3.1V, I_S=1.5A$	27	36	48	
		$V_{GS}=2.5V, I_S=1.5A$	31	42	55	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{SS}=V_{GS}, I_S=250\mu A$	0.5	0.65	1.2	V
I_{SSS}	Zero Gate Voltage Source Current	$V_{SS}=20V, V_{GS}=0V$	---	---	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 8V, V_{SS}=0V$	---	---	± 10	μA
G_{fs}	Forward Transconductance	$V_{SS}=10V, I_D=3.0A$	---	5.2	---	S
Q_g	Total Gate Charge ³	$V_{SS}=15V, V_{GS}=4.5V, I_S=6A$	---	10.4	---	nC
$T_{d(on)}$	Turn-On Delay Time ³	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega$ $I_S=3A$	---	3.2	---	ns
T_r	Rise Time ³		---	9.8	---	
$T_{d(off)}$	Turn-Off Delay Time ³		---	31	---	
T_f	Fall Time ³		---	3.6	---	
V_{FSS}	Forward Source-Source Voltage	$V_{GS}=0V, I_S=1.5A$	---	0.72	1.1	V

Note :

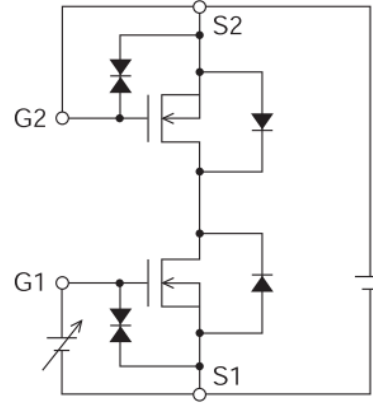
- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 10\mu s$, duty cycle $\leq 1\%$
- 3.Guaranteed by design, not subject to production testing.

Test circuits are example of measuring FET1 sides
Test Circuit 1 V_{SSS} / I_{SSS}

Test Circuit 2 $I_{GSS(+)} / (-)$


Test Circuit 3 $V_{GS(off)}$

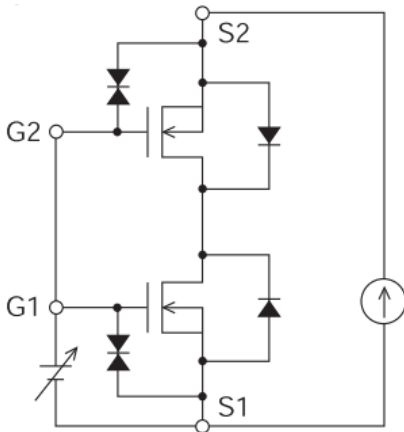


Test Circuit 4 G_{fs}

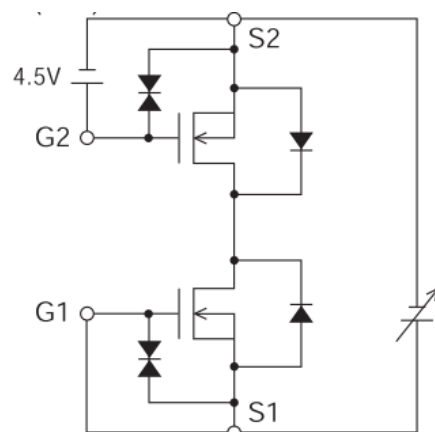


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

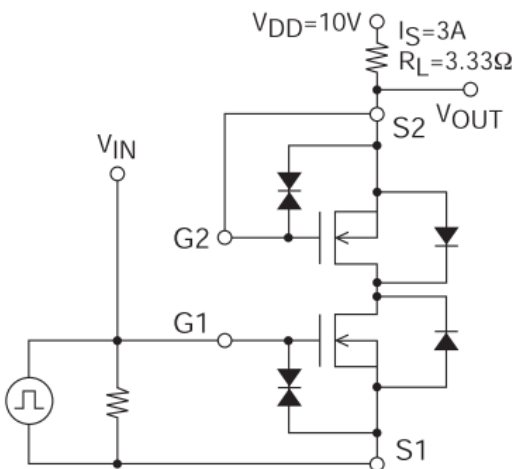
Test Circuit 5 $R_{SS(ON)}$



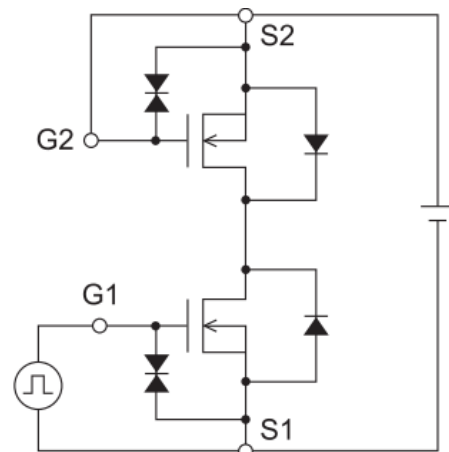
Test Circuit 6 $V_{F(S-S)}$



Test Circuit 7 $T_d(on)$, T_r , $T_d(off)$, T_f



Test Circuit 8 Q_g



* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

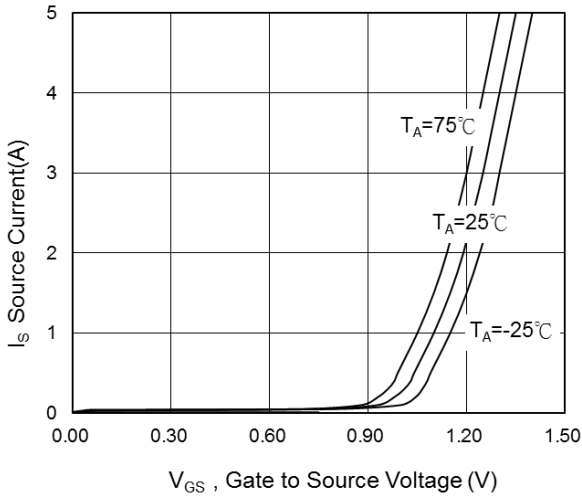


Fig.1 I_S - V_{GS}

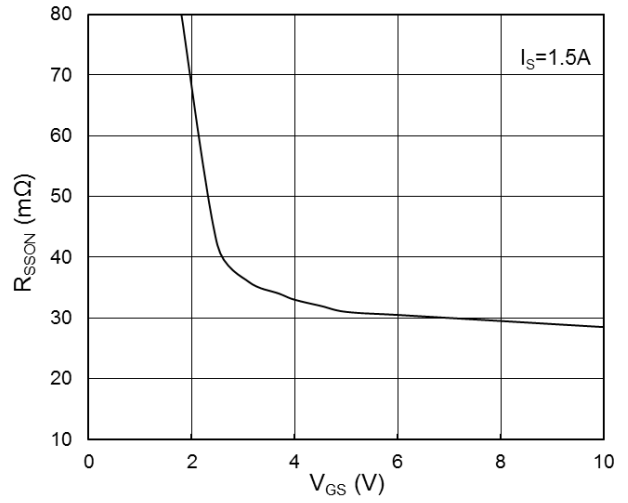


Fig.2 $R_{SS(ON)}$ - V_{GS}

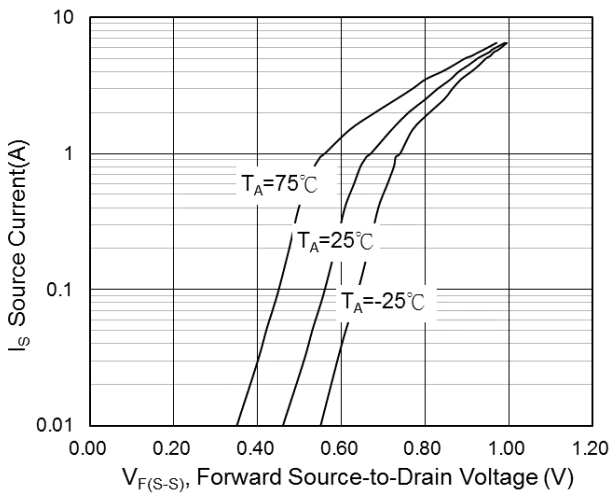


Fig.3 I_S - $V_{F(S-S)}$

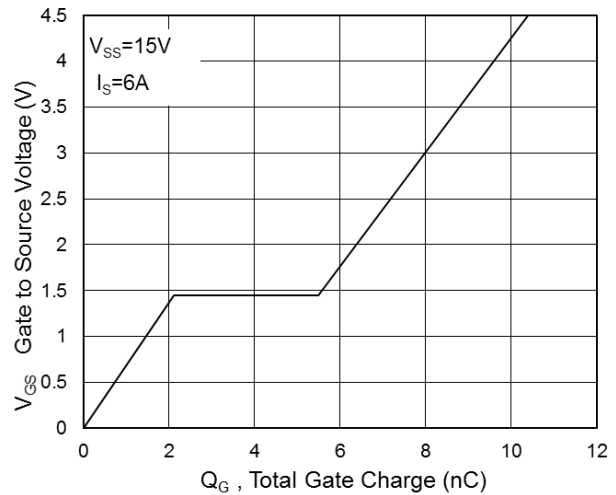


Fig.4 V_{GS} - Q_g

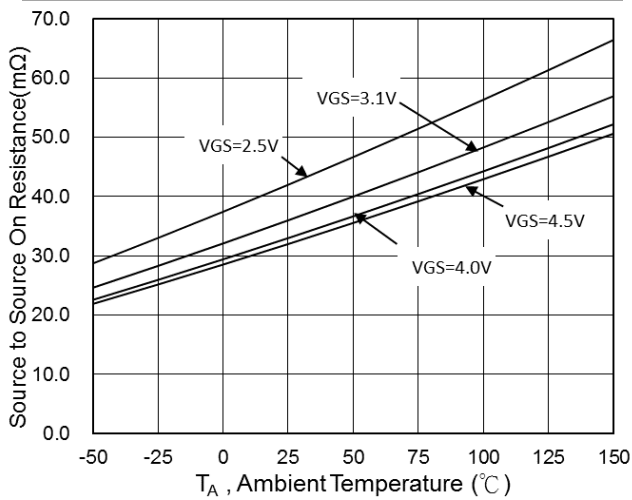


Fig.5 $R_{SS(ON)}$ - T_A

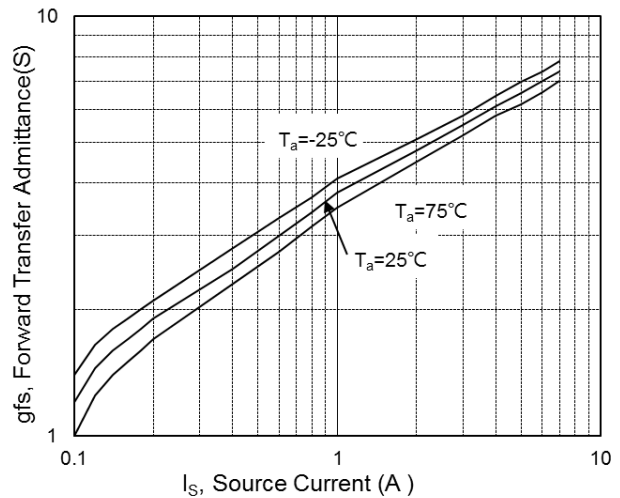


Fig.6 g_{fs} vs I_S

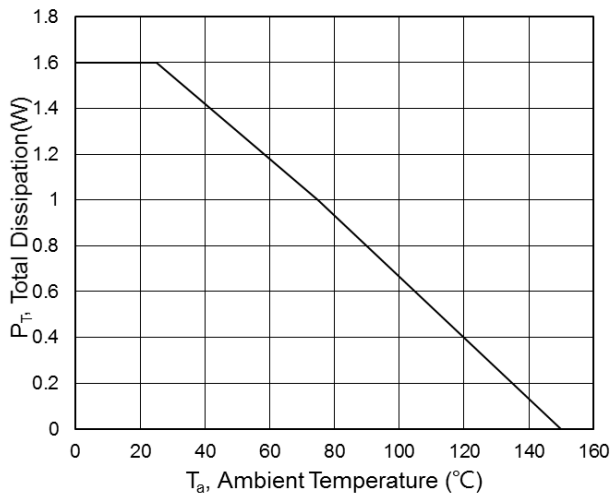


Fig.7 P_T - T_A

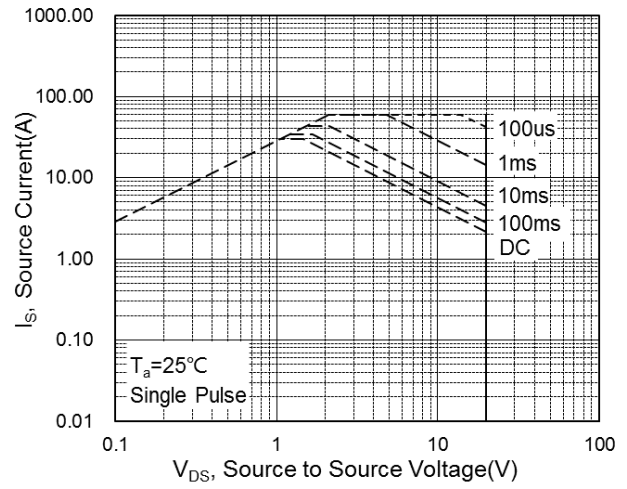


Fig.8 Safe Operating Area