



- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

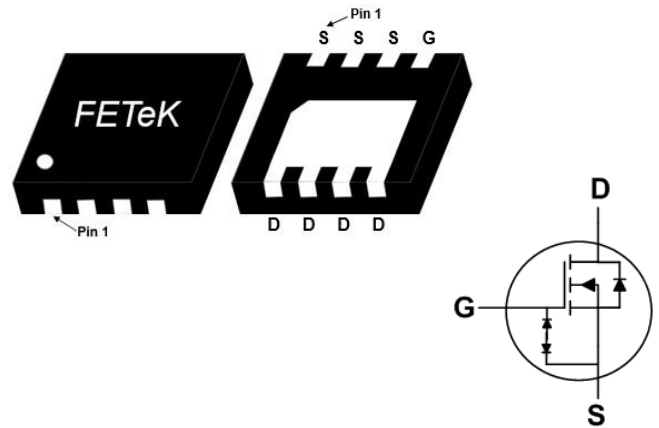
**Product Summary**

BVDSS	RDSON	ID
20V	2mΩ	50A

**Description**

The FKCE2530 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The FKCE2530 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

**DFN3.3x3.3 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current <sup>1</sup>	50	A
$I_D@T_C=100^\circ C$	Continuous Drain Current <sup>1</sup>	39	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	200	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	80	mJ
$I_{AS}$	Avalanche Current	40	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	83	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup> ( $t \leq 10S$ )	---	20	$^\circ C/W$
	Thermal Resistance Junction-ambient <sup>1</sup> (Steady State)	---	55	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-case <sup>1</sup>	---	1.5	$^\circ C/W$

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=4.5V, I_D=20A$	1.05	1.5	2	m $\Omega$
		$V_{GS}=2.5V, I_D=20A$	1.4	2	2.7	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.4	---	1.0	V
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	$\mu A$
		$V_{DS}=16V, V_{GS}=0V, T_J=125^\circ\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 10V, V_{DS}=0V$	---	---	$\pm 10$	$\mu A$
$R_g$	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.2	---	$\Omega$
$Q_g$	Total Gate Charge (10V)	$V_{DS}=15V, V_{GS}=10V, I_D=20A$	---	77	---	nC
$Q_{gs}$	Gate-Source Charge		---	8.7	---	
$Q_{gd}$	Gate-Drain Charge		---	14	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3\Omega, I_D=20A$	---	10.2	---	ns
$T_r$	Rise Time		---	11.7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	56.4	---	
$T_f$	Fall Time		---	16.2	---	
$C_{iss}$	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHz}$	---	4307	---	$\mu F$
$C_{oss}$	Output Capacitance		---	501	---	
$C_{rss}$	Reverse Transfer Capacitance		---	321	---	

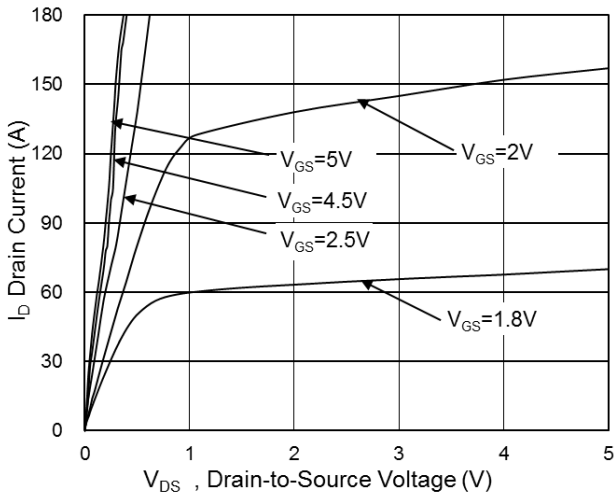
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,5</sup>	$V_G=V_D=0V$ , Force Current	---	---	50	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=20A, di/dt=100A/\mu s,$	---	22	---	nS
$Q_{rr}$	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	72	---	nC

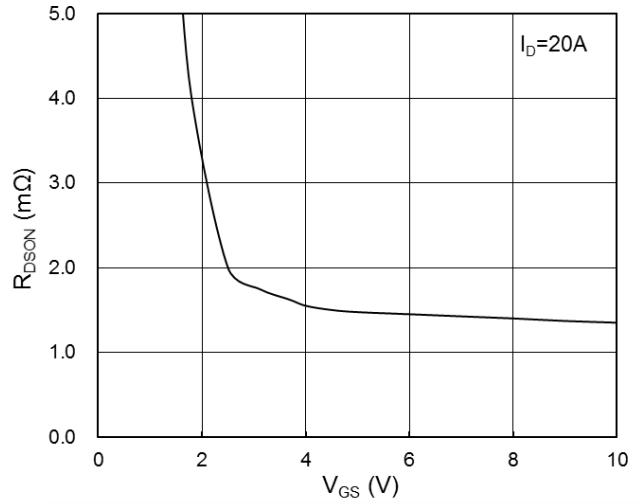
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=40A$
- 4.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 5.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

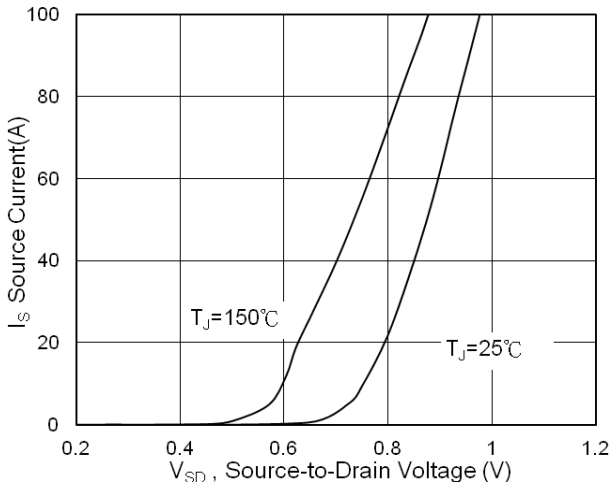
**Typical Characteristics**



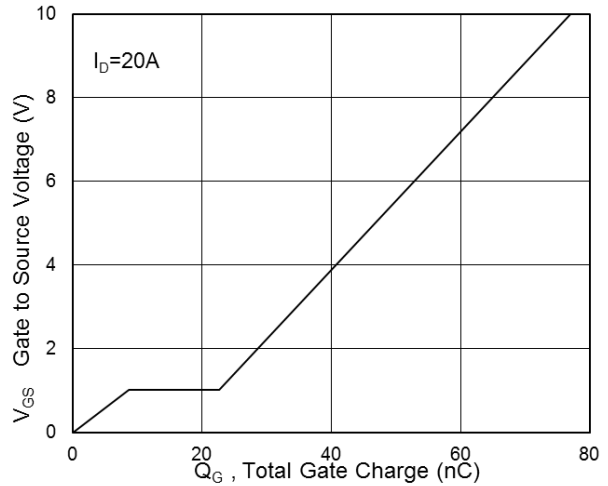
**Fig.1 Typical Output Characteristics**



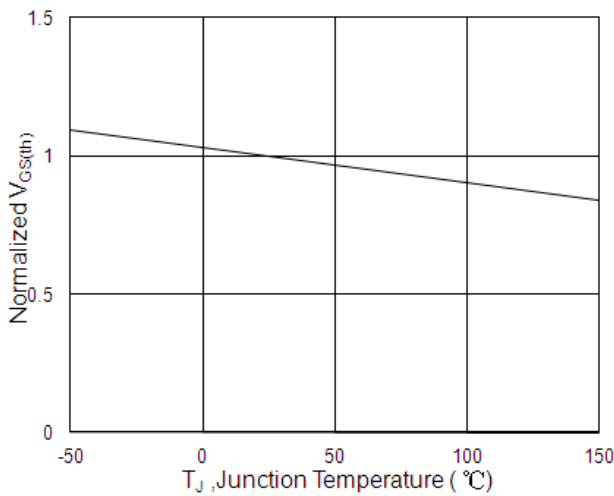
**Fig.2 On-Resistance vs. Gate-Source Voltage**



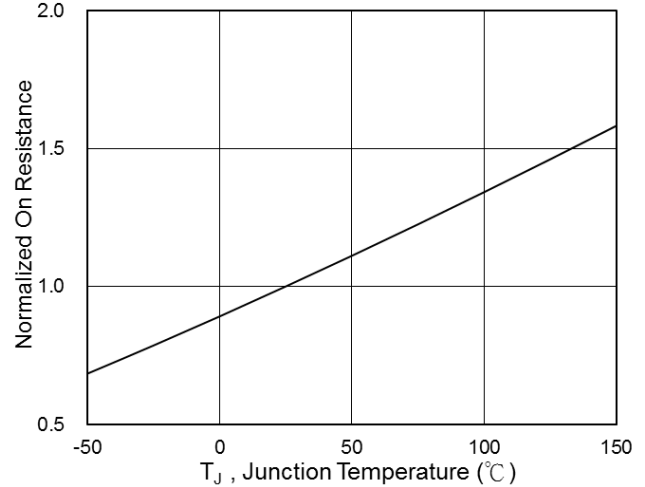
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

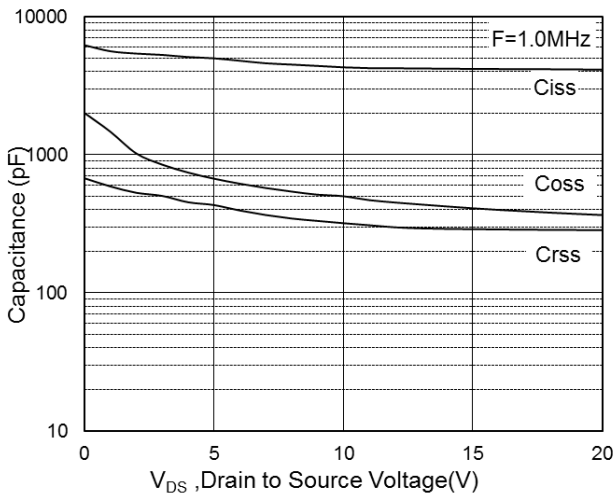


Fig.7 Capacitance

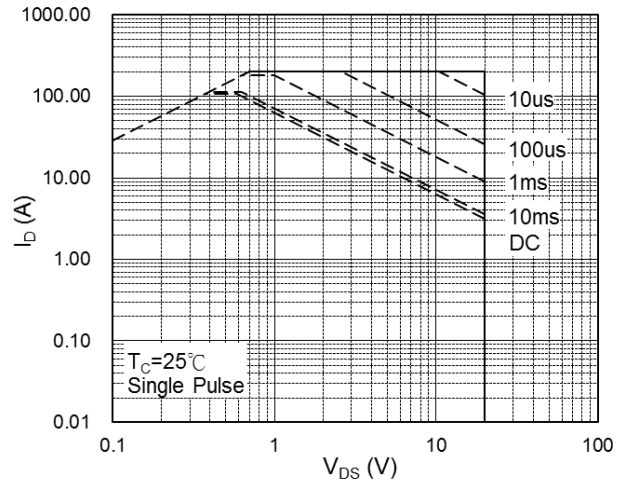


Fig.8 Safe Operating Area

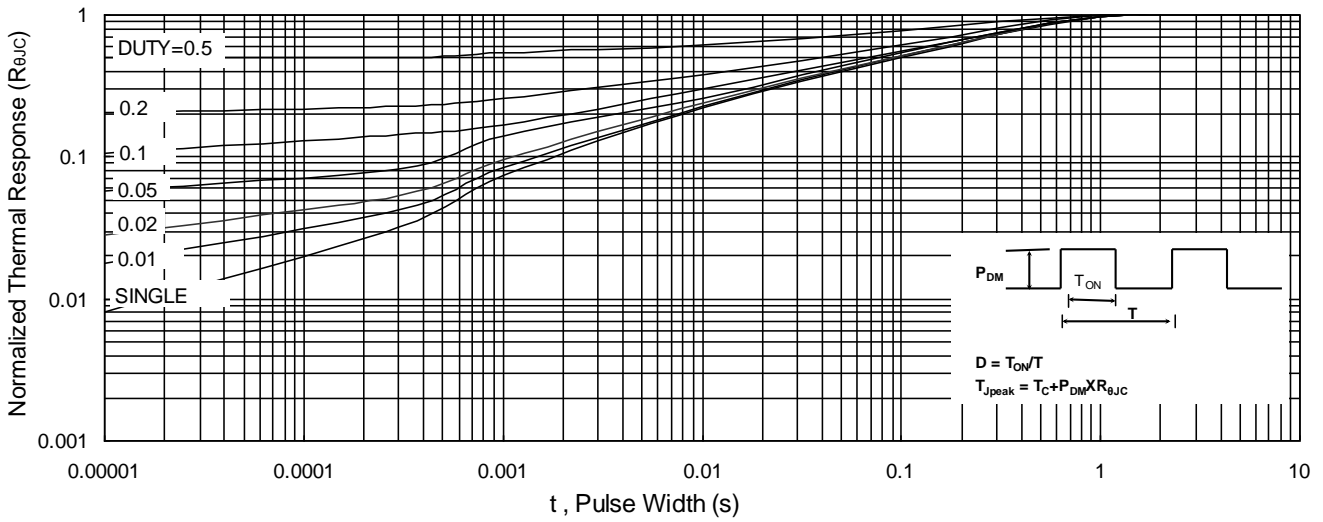


Fig.9 Normalized Maximum Transient Thermal Impedance

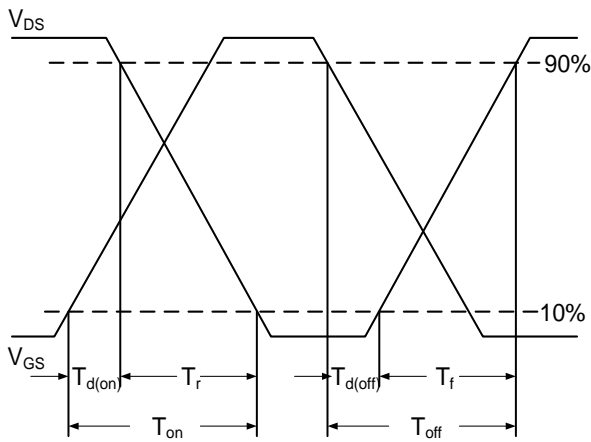


Fig.10 Switching Time Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

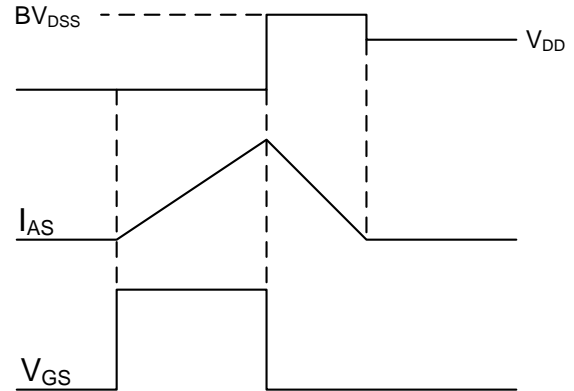
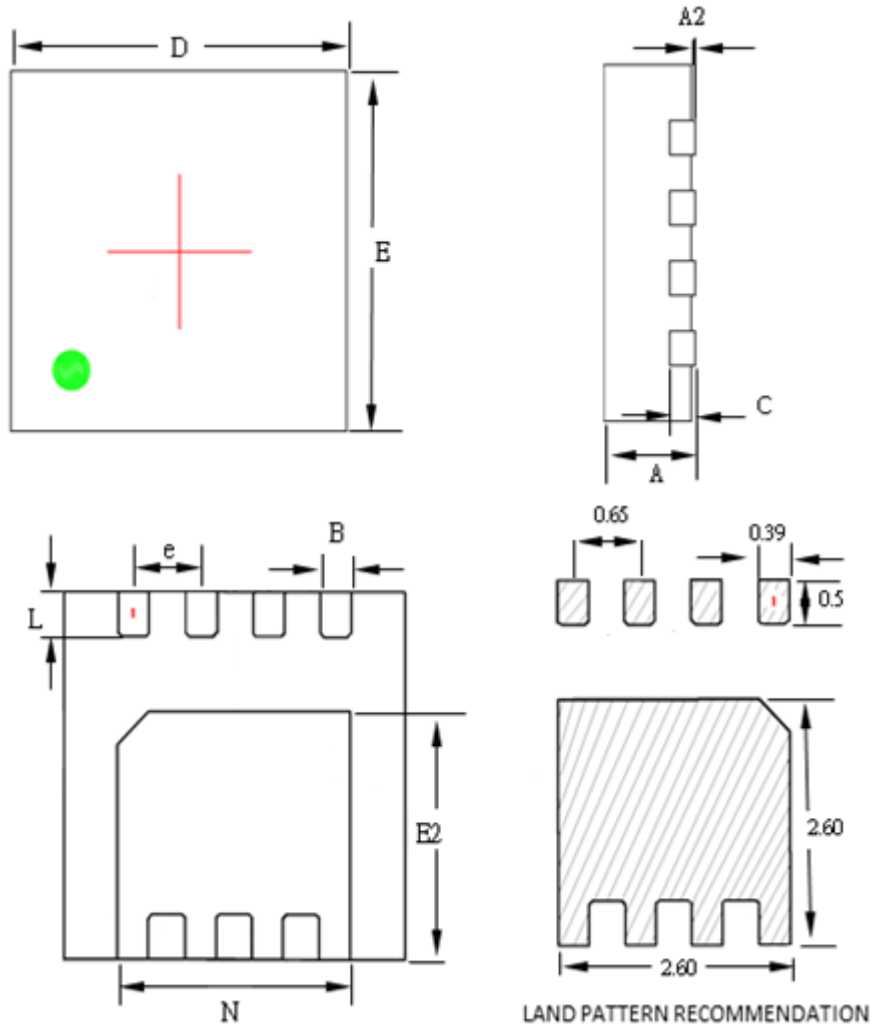


Fig.11 Unclamped Inductive Switching Waveform

**DFN3.3x3.3 8L Outline**


SYMBOLS	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A2	0.00	--	0.05	0.000	--	0.002
B	0.24	0.30	0.35	0.009	0.012	0.014
C	0.10	0.15	0.25	0.004	0.006	0.010
D	3.15	3.30	3.40	0.124	0.130	0.134
E	3.15	3.30	3.40	0.124	0.130	0.134
E2	2.15	2.25	2.35	0.085	0.089	0.093
L	0.35	0.40	0.45	0.014	0.016	0.018
N	2.10	2.25	2.35	0.083	0.089	0.093
e	--	0.65	--	--	0.026	--