

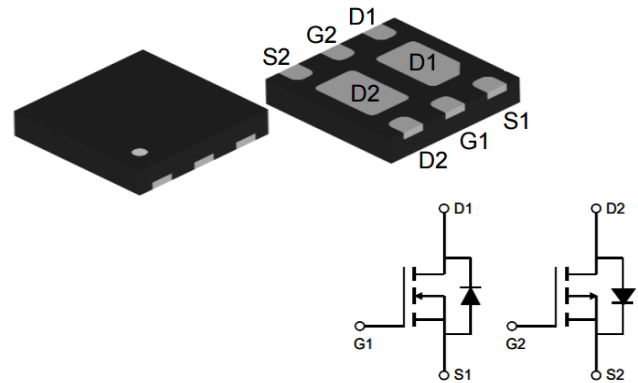
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent Cdv/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary


BVDSS	RDSON	ID
20V	40mΩ	5A
-20V	100mΩ	-4.5A

Description

The FKCB2903 is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDSON and gate charge for most of the small power switching and load switch applications. The FKCB2903 meet the RoHS and Green Product requirement with full function reliability approved.

DFN2X2 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
		Steady State	Steady State	
V _{DS}	Drain-Source Voltage	20	-20	V
V _{GS}	Gate-Source Voltage	±12	±12	V
I _D @T _C =25°C	Continuous Drain Current ¹	5	-4.5	A
I _D @T _C =70°C	Continuous Drain Current ¹	4.2	-3.7	A
I _{DM}	Pulsed Drain Current ²	15	-12	A
P _D @T _A =25°C	Total Power Dissipation ³	1.56	1.56	W
P _D @T _C =25°C	Total Power Dissipation ³	8.3	8.3	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	80	°C/W
R _{θJC}	Thermal Resistance Junction-ambient ¹	---	15	°C/W

**Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=4.5V, I_D=3A$	---	28	40	m Ω
		$V_{GS}=2.5V, I_D=2A$	---	37	55	
		$V_{GS}=1.8V, I_D=1.5A$	---	51	70	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	0.4	---	1.0	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=16V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=3A$	---	10.5	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=3A$	---	4.6	---	nC
Q_{gs}	Gate-Source Charge		---	0.7	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V, V_{GS}=4.5V, R_G=3.3\Omega$ $I_D=3A$	---	1.6	---	ns
T_r	Rise Time		---	42	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14	---	
T_f	Fall Time		---	7	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	310	---	μF
C_{oss}	Output Capacitance		---	49	---	
C_{rss}	Reverse Transfer Capacitance		---	35	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	1.5	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150 $^\circ\text{C}$ junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

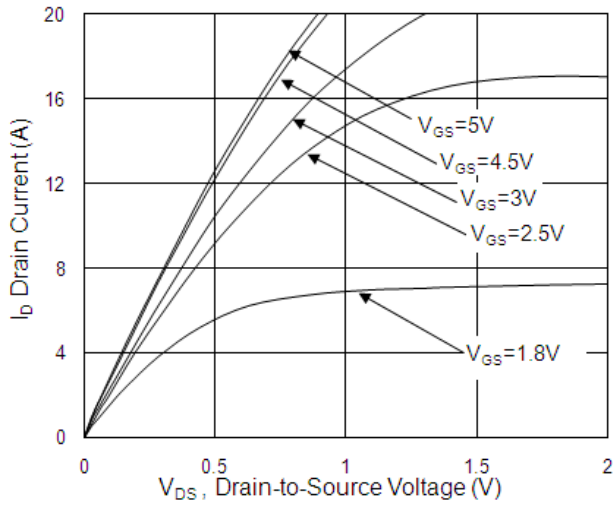


Fig.1 Typical Output Characteristics

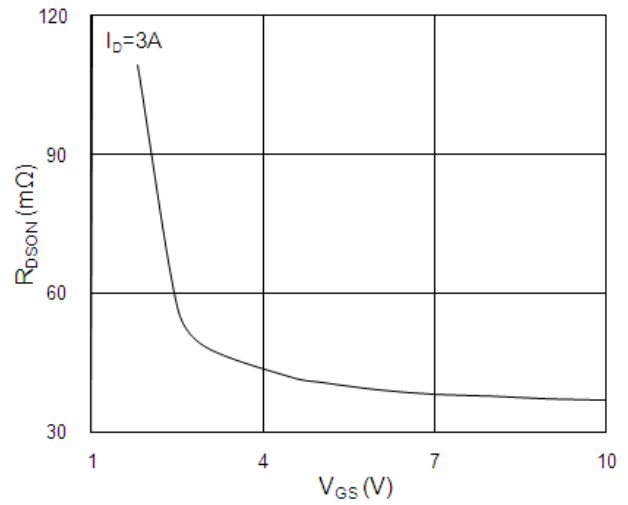


Fig.2 On-Resistance vs G-S Voltage

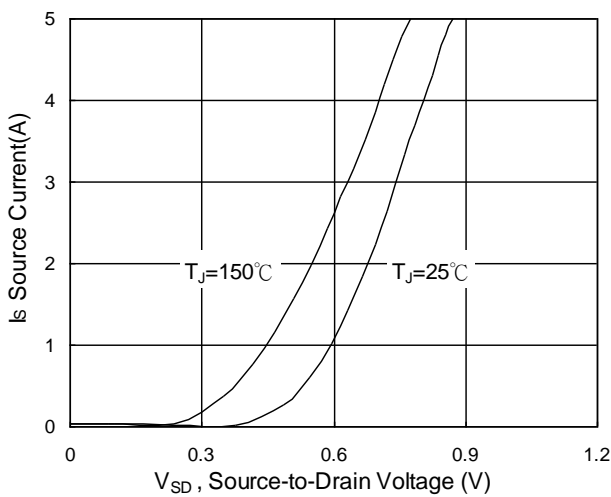


Fig.3 Source Drain Forward Characteristics

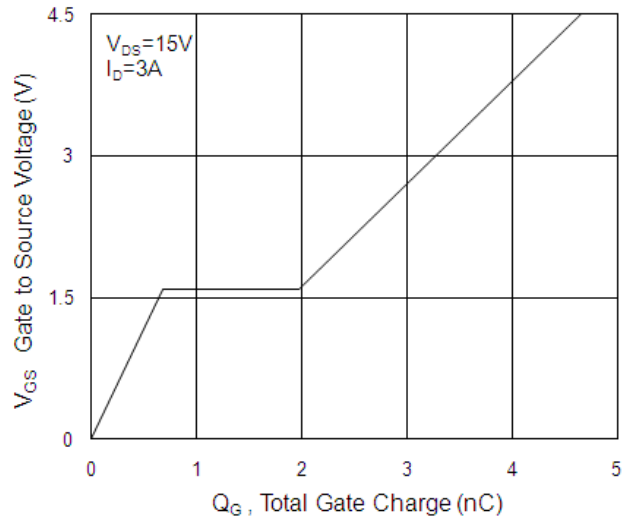


Fig.4 Gate-Charge Characteristics

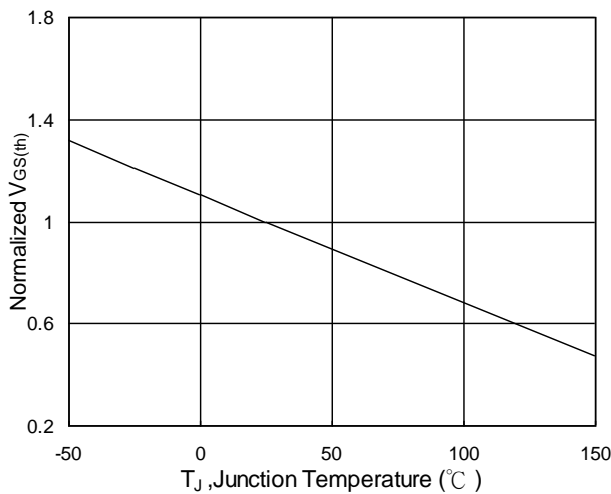


Fig.5 Normalized $V_{GS(th)}$ vs T_J

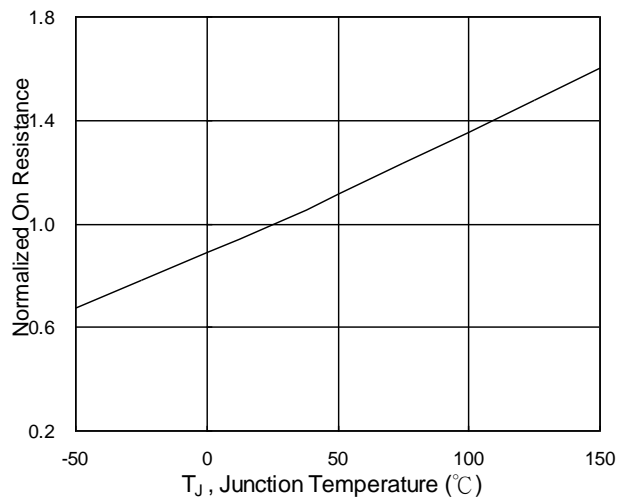


Fig.6 Normalized $R_{DS(on)}$ vs T_J

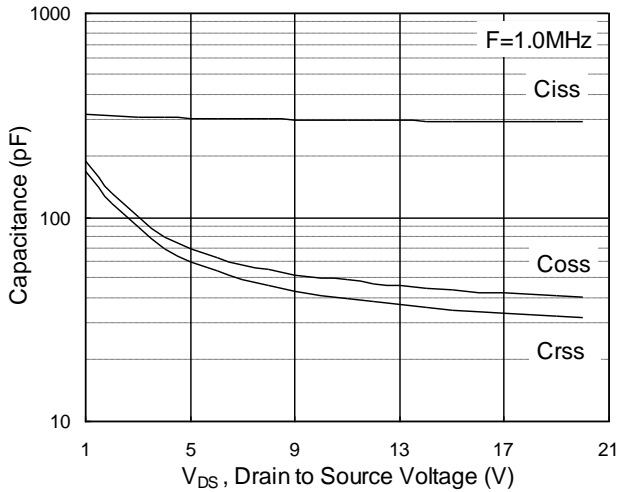


Fig.7 Capacitance

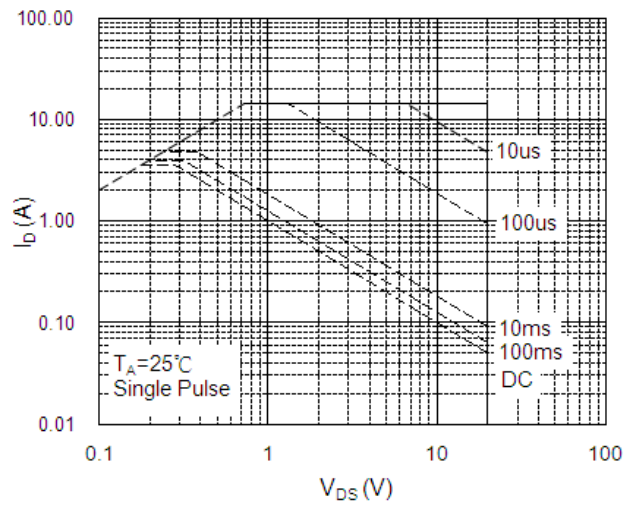


Fig.8 Safe Operating Area

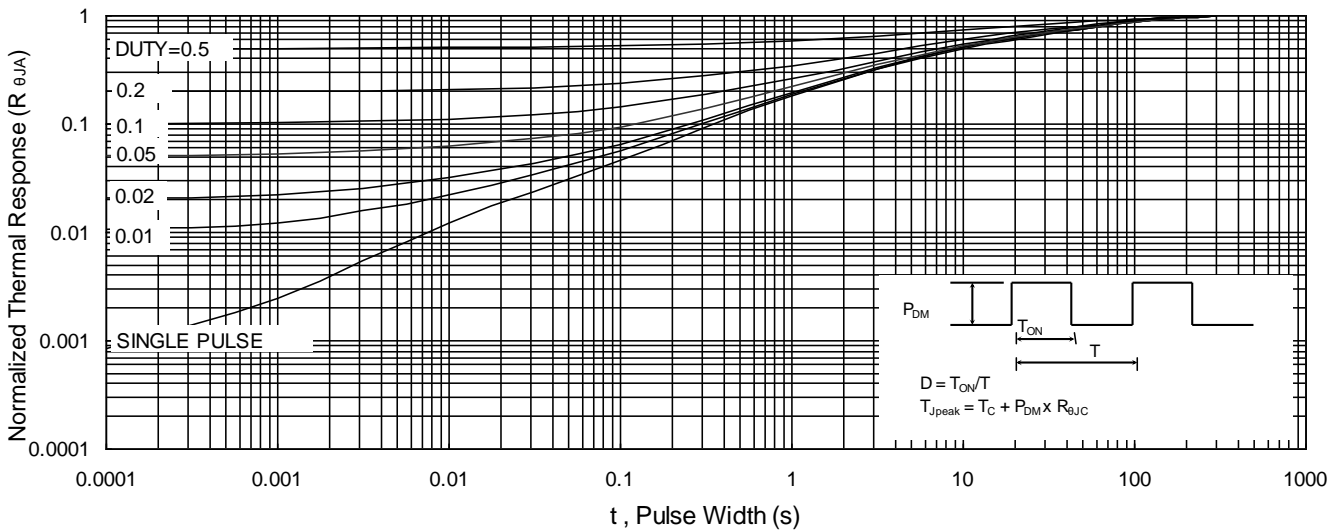


Fig.9 Normalized Maximum Transient Thermal Impedance

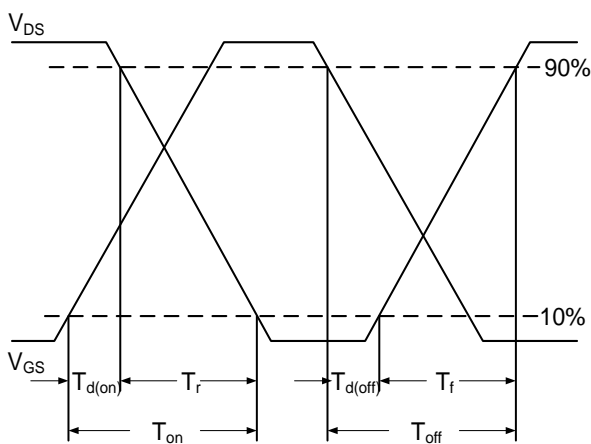


Fig.10 Switching Time Waveform

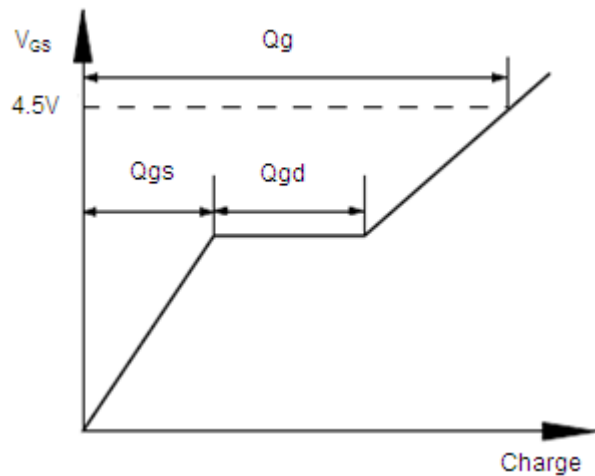


Fig.11 Gate Charge Waveform

**Electrical Characteristics (T_J=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-20	---	---	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-3A	---	85	100	mΩ
		V _{GS} =-2.5V, I _D =-1.5A	---	125	145	
		V _{GS} =-1.8V, I _D =-0.5A	---	170	200	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-0.4	---	-1.0	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-16V, V _{GS} =0V, T _J =25°C	---	---	-1	uA
		V _{DS} =-16V, V _{GS} =0V, T _J =55°C	---	---	-5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-3A	---	12.2	---	S
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-3A	---	10.1	---	nC
Q _{gs}	Gate-Source Charge		---	1.21	---	
Q _{gd}	Gate-Drain Charge		---	2.46	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-10V, V _{GS} =-4.5V, R _G =3.3Ω I _D =-3A	---	5.6	---	ns
T _r	Rise Time		---	32.2	---	
T _{d(off)}	Turn-Off Delay Time		---	45.6	---	
T _f	Fall Time		---	29.2	---	
C _{iSS}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	677	---	pF
C _{oss}	Output Capacitance		---	82	---	
C _{rSS}	Reverse Transfer Capacitance		---	73	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-1.5	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1	V

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

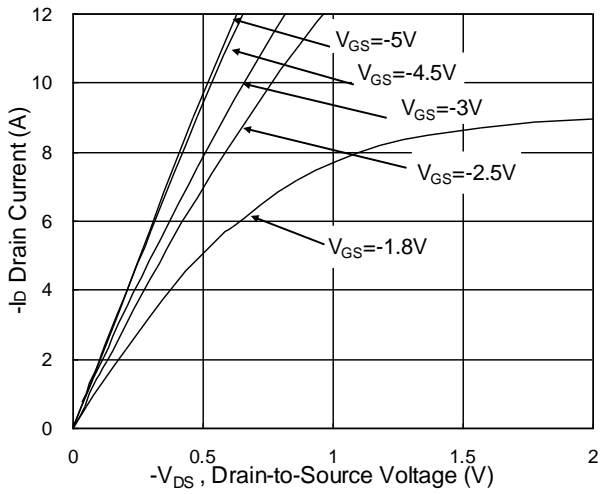


Fig.1 Typical Output Characteristics

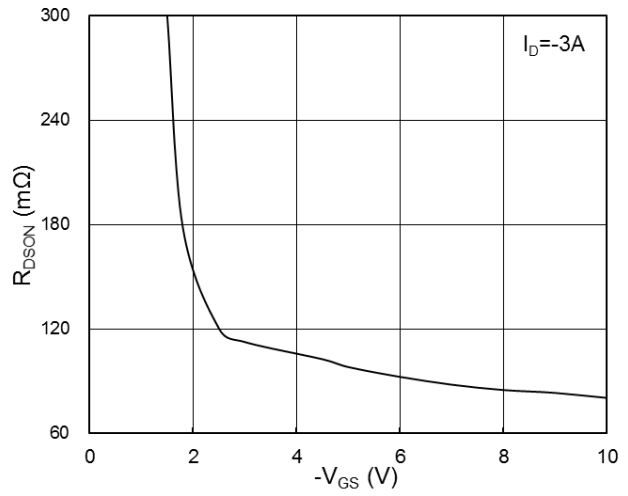


Fig.2 On-Resistance vs G-S Voltage

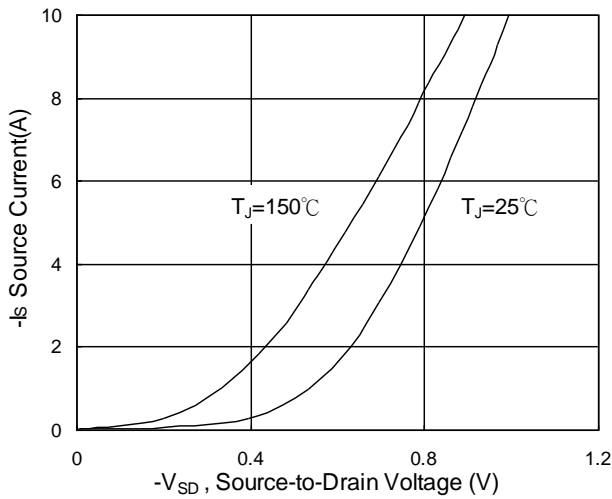


Fig.3 Source Drain Forward Characteristics

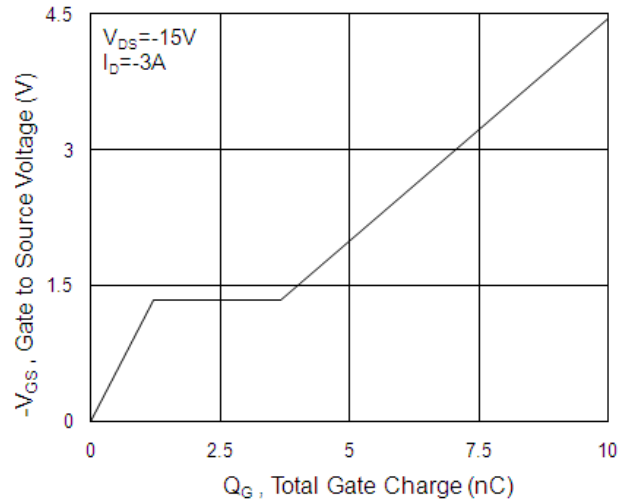


Fig.4 Gate-Charge Characteristics

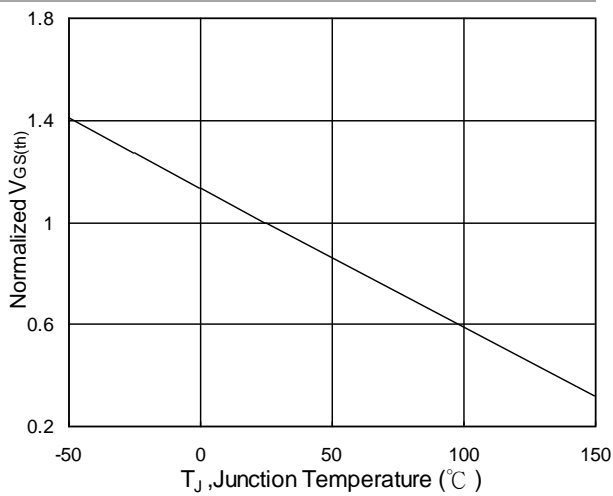


Fig.5 Normalized $V_{GS(th)}$ vs T_J

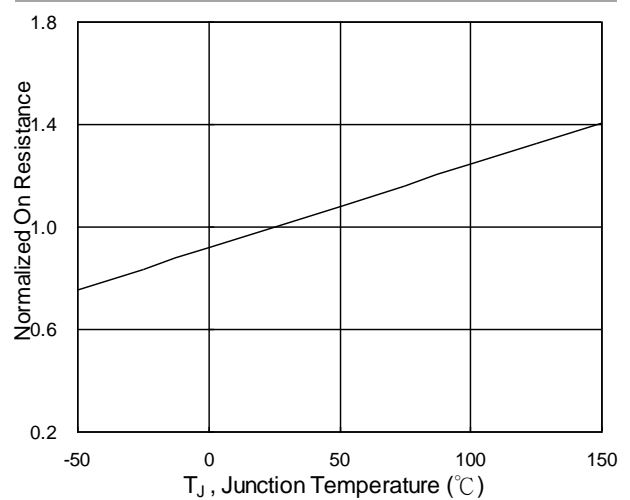


Fig.6 Normalized $R_{DS(on)}$ vs T_J

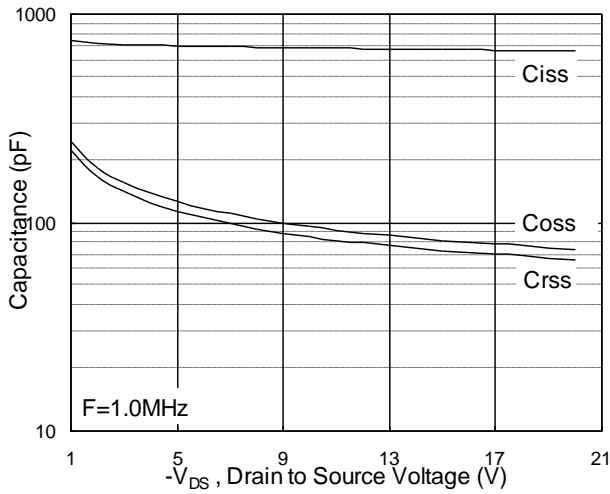


Fig.7 Capacitance

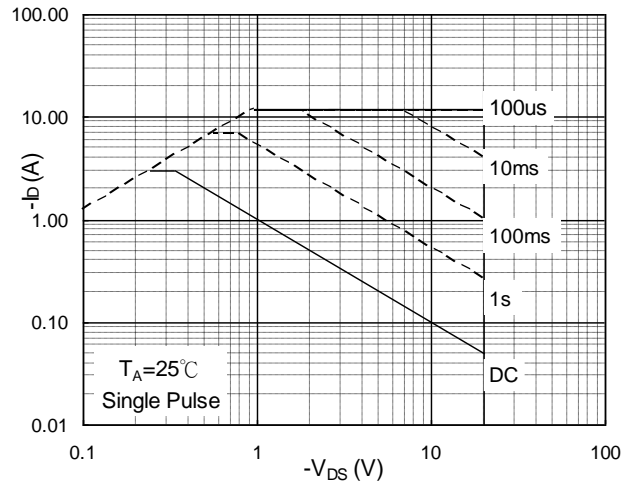


Fig.8 Safe Operating Area

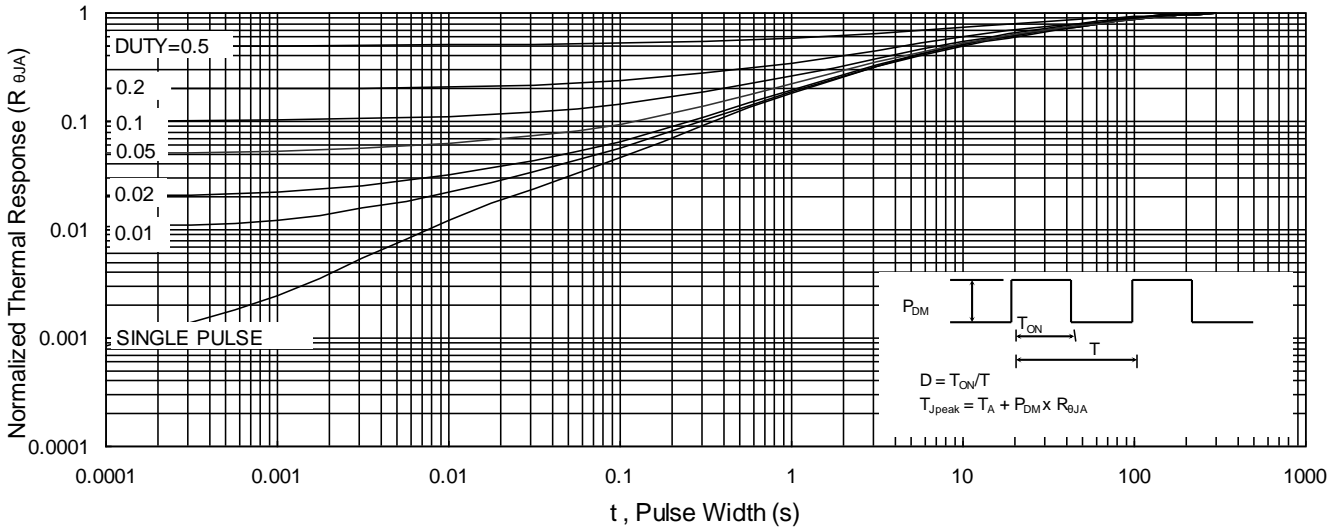


Fig.9 Normalized Maximum Transient Thermal Impedance

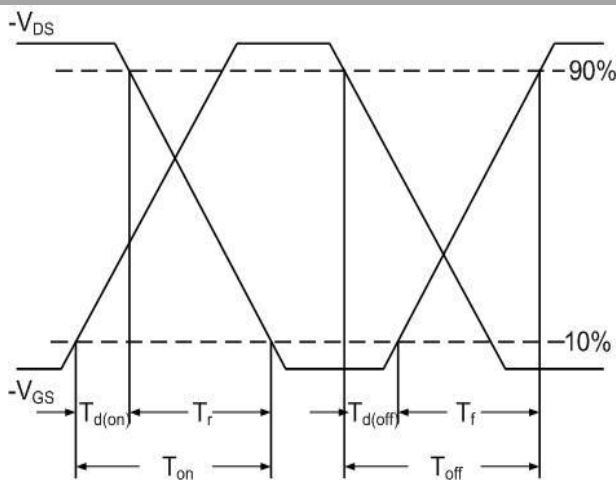


Fig.10 Switching Time Waveform

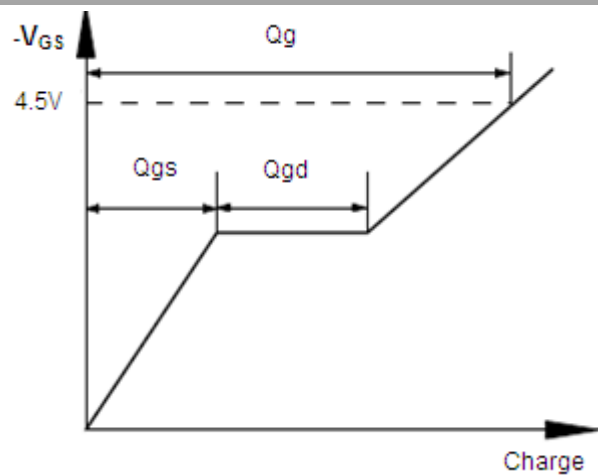
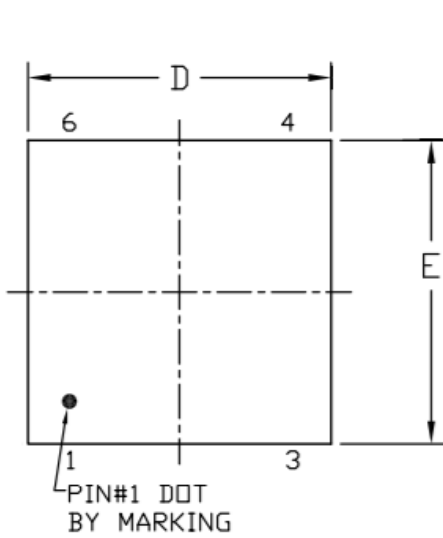
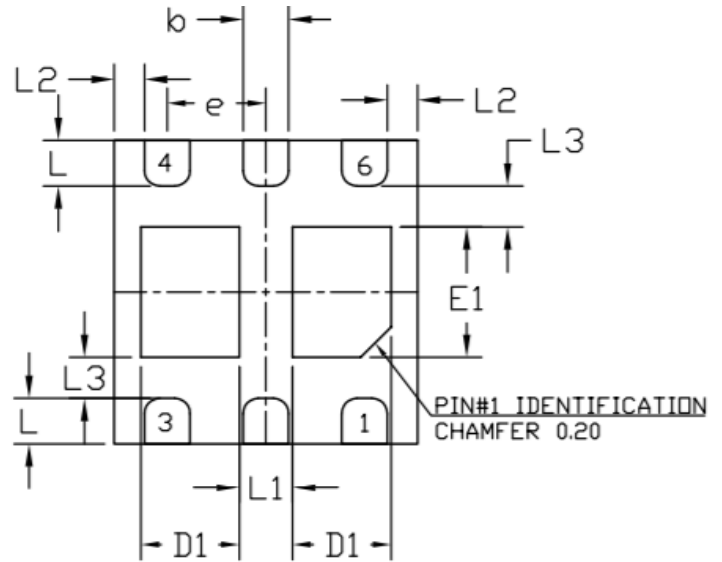


Fig.11 Gate Charge Waveform

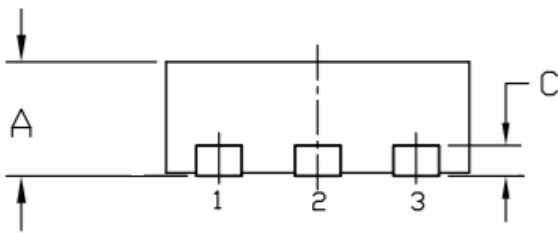
DFN2X2 Package Outline Dimensions



TOP VIEW

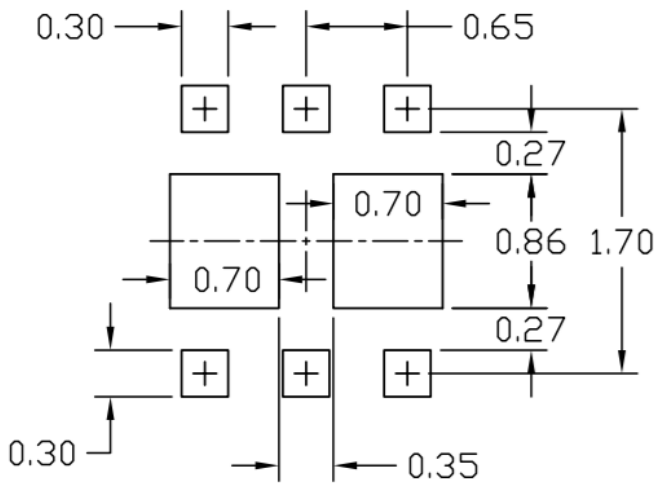


BOTTOM VIEW



FRONT VIEW

RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.20 Ref.			0.008 Ref.		
D	1.90	2.00	2.10	0.075	0.079	0.083
D1	0.620	0.650	0.680	0.024	0.026	0.027
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	0.76	0.86	0.96	0.030	0.034	0.038
e	0.65 BSC			0.026 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
L1	0.320	0.350	0.380	0.013	0.014	0.015
L2	0.170	0.200	0.230	0.007	0.008	0.009
L3	0.240	0.270	0.300	0.009	0.011	0.012