

- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

Product Summary



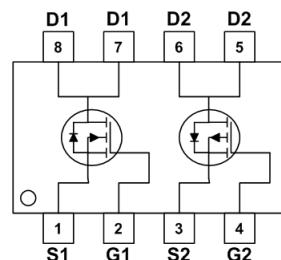
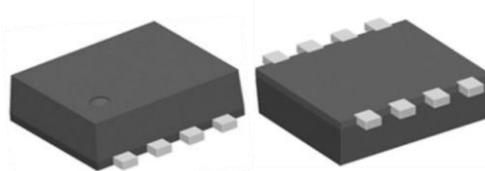
BVDSS	RDS(on)	ID
100V	310mΩ	2A
-100V	650mΩ	-1.5A

General Description

The FKBE0901 is the high cell density trenched N-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The FKBE0901 meet the RoHS and Green Product requirement with full function reliability approved.

PRPAK3X3 NEP Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
V _{DS}	Drain-Source Voltage	100	-100	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	2	1.5	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	1.7	1.2	A
I _{DM}	Pulsed Drain Current ²	3	3	A
P _D @T _A =25°C	Total Power Dissipation ³	1.5	1.5	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	85	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	60	°C/W

N-Channel Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	100	---	---	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{GS}=10\text{V}$, $I_D=1.5\text{A}$	---	260	310	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}$, $I_D=1\text{A}$	---	270	320	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	1.2	1.7	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	10	uA
		$V_{DS}=80\text{V}$, $V_{GS}=0\text{V}$, $T_J=55\text{ }^{\circ}\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=1.5\text{A}$	---	5.36	---	S
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=1.5\text{A}$	---	4	---	nC
Q_{gs}	Gate-Source Charge		---	1.2	---	
Q_{gd}	Gate-Drain Charge		---	1.3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $R_G=3.3\Omega$	---	5.2	---	ns
T_r	Rise Time		---	7	---	
$T_{d(off)}$	Turn-Off Delay Time		---	14.8	---	
T_f	Fall Time		---	2	---	
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	508	---	pF
C_{oss}	Output Capacitance		---	29	---	
C_{rss}	Reverse Transfer Capacitance		---	16	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	1	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_s=1\text{A}$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by $150\text{ }^{\circ}\text{C}$ junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$	-100	---	---	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10\text{V}$, $I_D=-1\text{A}$	---	0.52	0.65	Ω
		$V_{GS}=-4.5\text{V}$, $I_D=-0.5\text{A}$	---	0.56	0.7	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu\text{A}$	-1.2	-1.7	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-80\text{V}$, $V_{GS}=0\text{V}$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	10	μA
		$V_{DS}=-80\text{V}$, $V_{GS}=0\text{V}$, $T_J=55\text{ }^{\circ}\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5\text{V}$, $I_D=-1\text{A}$	---	2.9	---	S
Q_g	Total Gate Charge (-10V)	$V_{DS}=-50\text{V}$, $V_{GS}=-10\text{V}$, $I_D=-1\text{A}$	---	9.3	---	nC
Q_{gs}	Gate-Source Charge		---	1.75	---	
Q_{gd}	Gate-Drain Charge		---	1.25	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-50\text{V}$, $V_{GS}=-10\text{V}$, $R_G=3.3\Omega$	---	2	---	ns
T_r	Rise Time		---	18.4	---	
$T_{d(off)}$	Turn-Off Delay Time		---	19.6	---	
T_f	Fall Time		---	19.6	---	
C_{iss}	Input Capacitance	$V_{DS}=-15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	---	553	---	pF
C_{oss}	Output Capacitance		---	29	---	
C_{rss}	Reverse Transfer Capacitance		---	20	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,4}	$V_G=V_D=0\text{V}$, Force Current	---	---	-1	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0\text{V}$, $I_s=-1\text{A}$, $T_J=25\text{ }^{\circ}\text{C}$	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.