

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

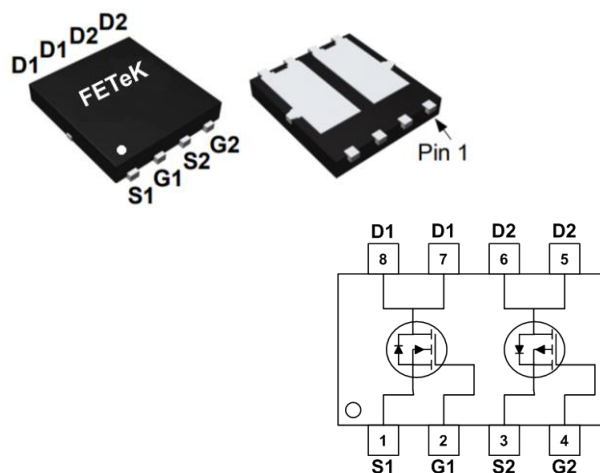
Product Summary


BVDSS	RDS(on)	ID
30V	12mΩ	33A
-30V	18mΩ	-31A

Description

The FKBA3905 is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The FKBA3905 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

PRPAK5X6 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V _{DS}	Drain-Source Voltage	30	-30	V
V _{GS}	Gate-Source Voltage	±20	±20	V
I _D @T _C =25°C	Continuous Drain Current ^{1,5}	33	-31	A
I _D @T _C =70°C	Continuous Drain Current ^{1,5}	21	-20	A
I _{DM}	Pulsed Drain Current ²	60	-60	A
EAS	Single Pulse Avalanche Energy ³	24	72	mJ
I _{AS}	Avalanche Current	22	-38	A
P _D @T _C =25°C	Total Power Dissipation ⁴	25	25	W
T _{STG}	Storage Temperature Range	-55 to 150	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	55	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	5	°C/W

**N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	30	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=9A$	---	9	12	$m\Omega$
		$V_{GS}=4.5V$, $I_D=5A$	---	12	18	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	---	2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=9A$	---	25	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	1.8	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V$, $V_{GS}=4.5V$, $I_D=9A$	---	9.8	---	nC
Q_{gs}	Gate-Source Charge		---	4.1	---	
Q_{gd}	Gate-Drain Charge		---	3.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V$, $V_{GS}=10V$, $R_G=1.5\Omega$ $I_D=1A$	---	4.1	---	ns
T_r	Rise Time		---	8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	29	---	
T_f	Fall Time		---	3.8	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	942	---	pF
C_{oss}	Output Capacitance		---	132	---	
C_{rss}	Reverse Transfer Capacitance		---	108	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^\circ\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=9A$, $dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	8.8	---	nS
Q_{rr}	Reverse Recovery Charge		---	3.6	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.1mH$, $I_{AS}=27A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

**P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)**

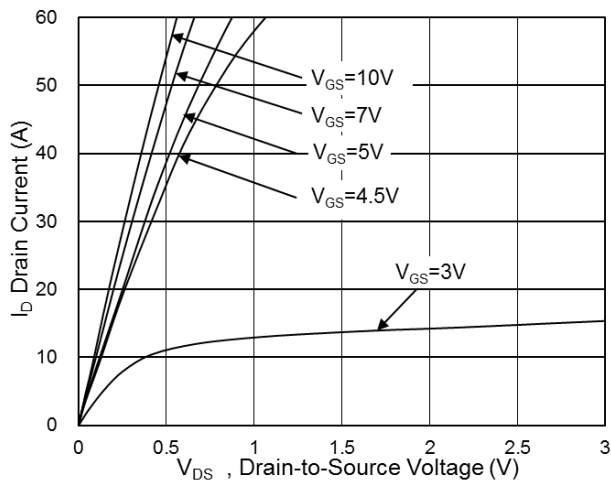
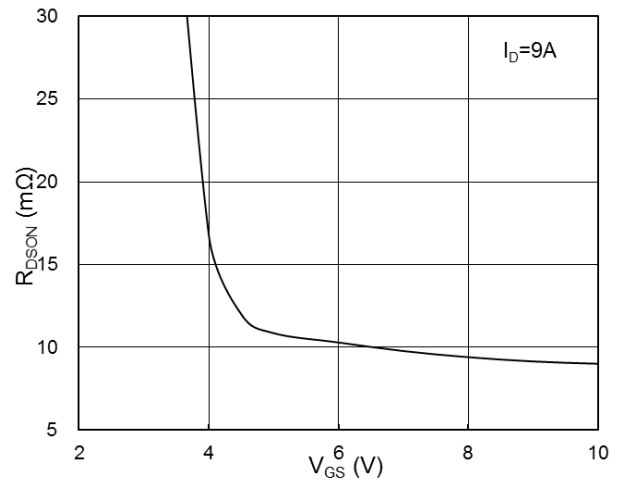
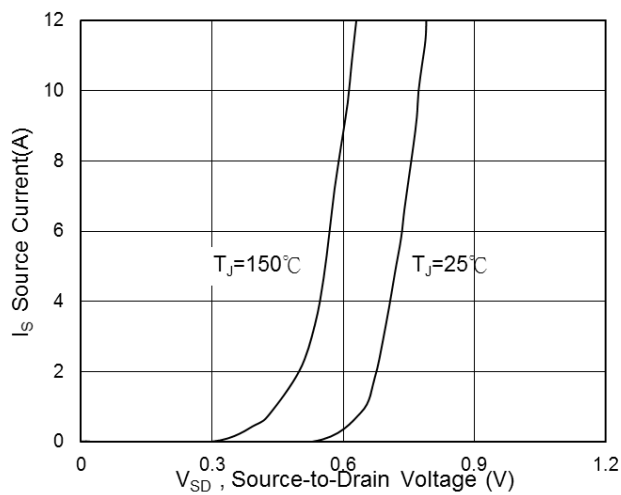
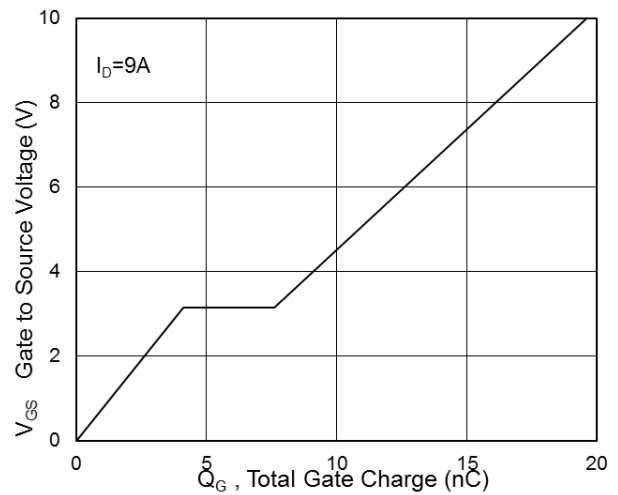
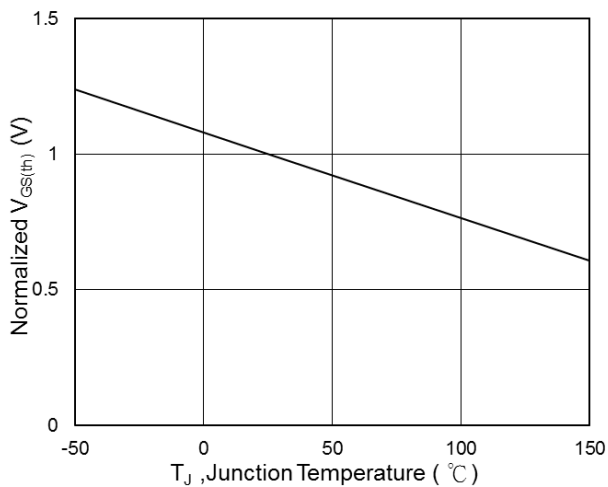
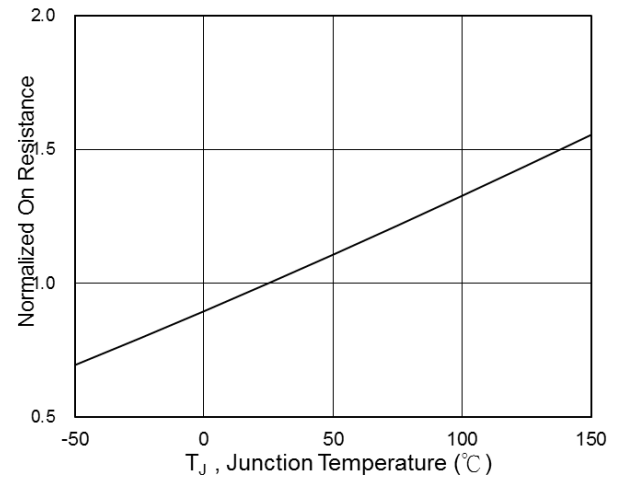
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-30	---	---	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V$, $I_D=-8A$	---	13	18	$m\Omega$
		$V_{GS}=-4.5V$, $I_D=-4A$	---	19	28	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-1.0	---	-2.5	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-24V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V$, $I_D=-8A$	---	24	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V$, $V_{GS}=-4.5V$, $I_D=-8A$	---	22	---	nC
Q_{gs}	Gate-Source Charge		---	5.4	---	
Q_{gd}	Gate-Drain Charge		---	7	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V$, $V_{GS}=-10V$, $R_G=3.3\Omega$ $I_D=-1A$	---	32	---	ns
T_r	Rise Time		---	34.5	---	
$T_{d(off)}$	Turn-Off Delay Time		---	71	---	
T_f	Fall Time		---	10.2	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	2213	---	pF
C_{oss}	Output Capacitance		---	311	---	
C_{rss}	Reverse Transfer Capacitance		---	235	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-6	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=-1A$, $T_J=25^\circ\text{C}$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F=-8A$, $dI/dt=100A/\mu s$, $T_J=25^\circ\text{C}$	---	17	---	nS
Q_{rr}	Reverse Recovery Charge		---	6.5	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=-25V$, $V_{GS}=-10V$, $L=0.1mH$, $I_{AS}=-56A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage

Fig.3 Source Drain Forward Characteristics

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J

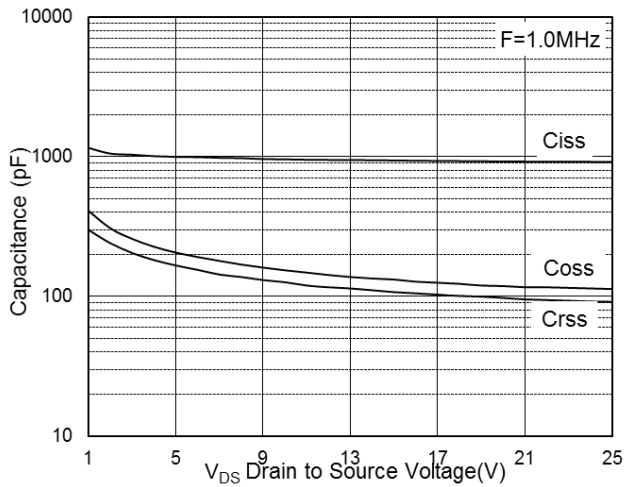


Fig.7 Capacitance

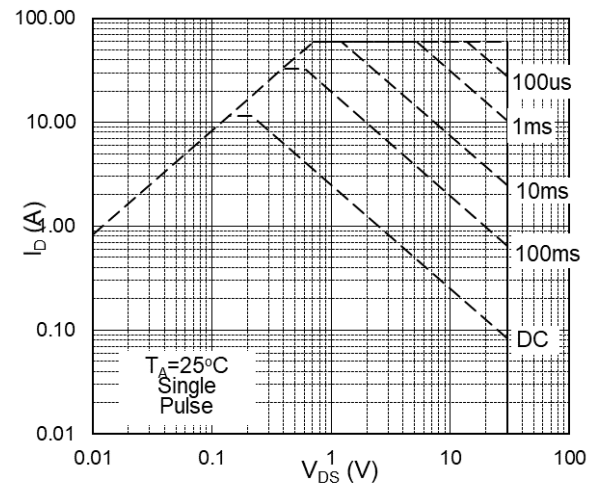


Fig.8 Safe Operating Area

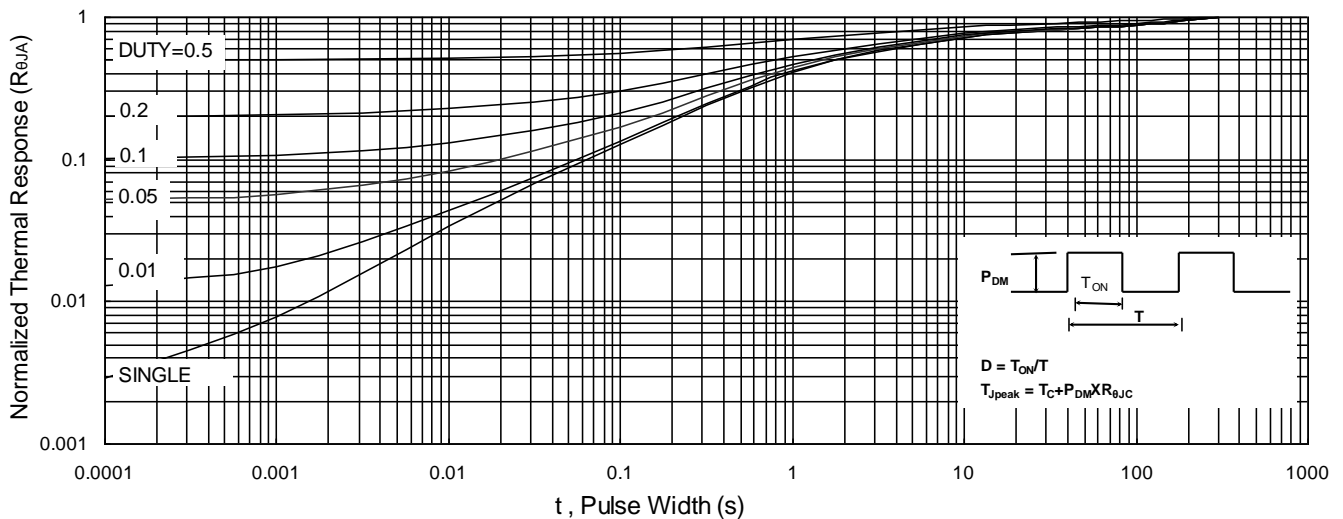


Fig.9 Normalized Maximum Transient Thermal Impedance

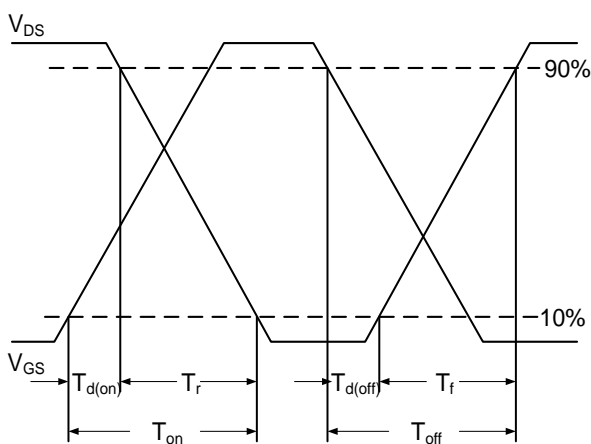


Fig.10 Switching Time Waveform

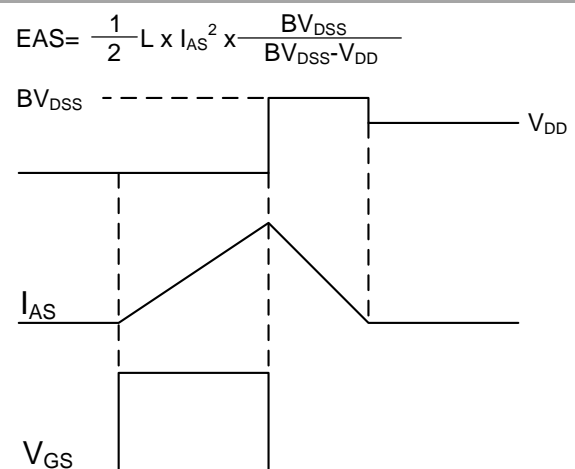
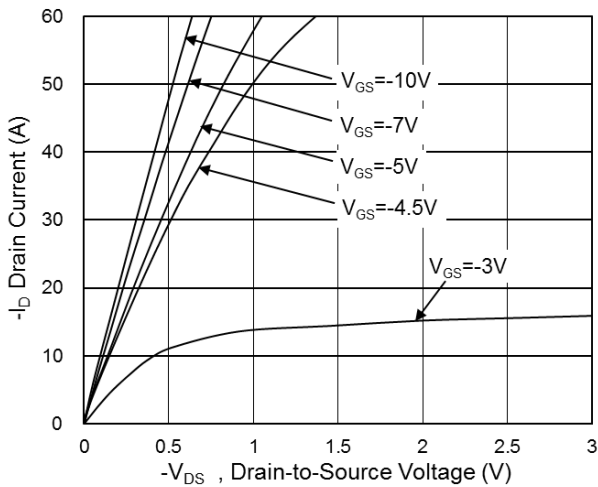
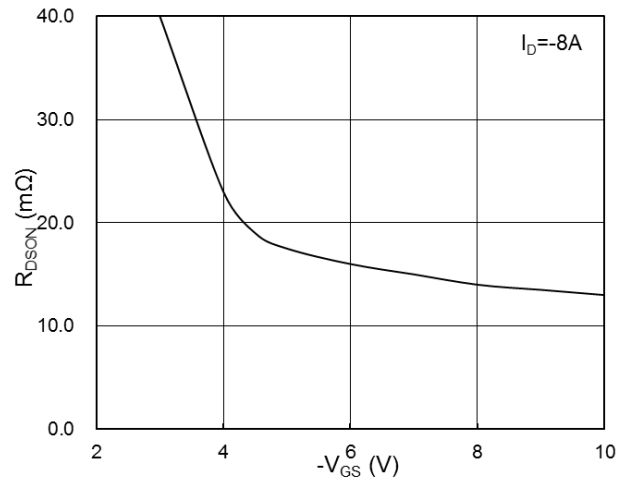
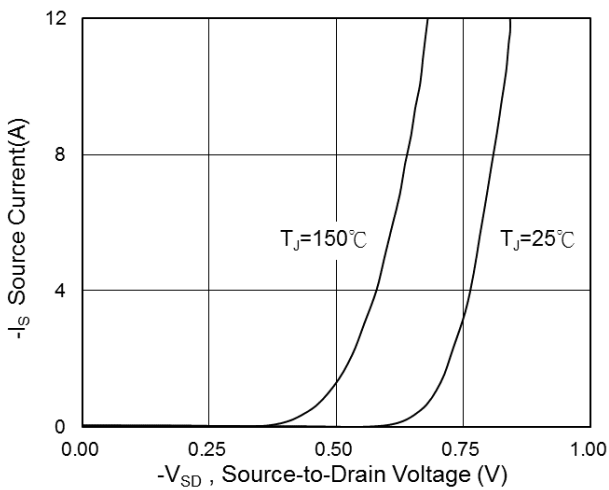
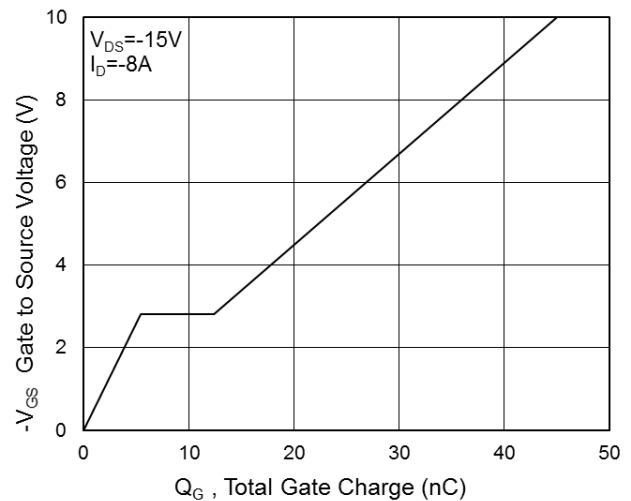
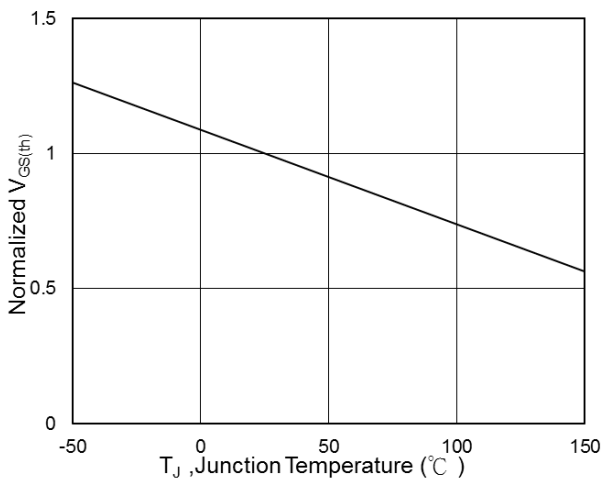
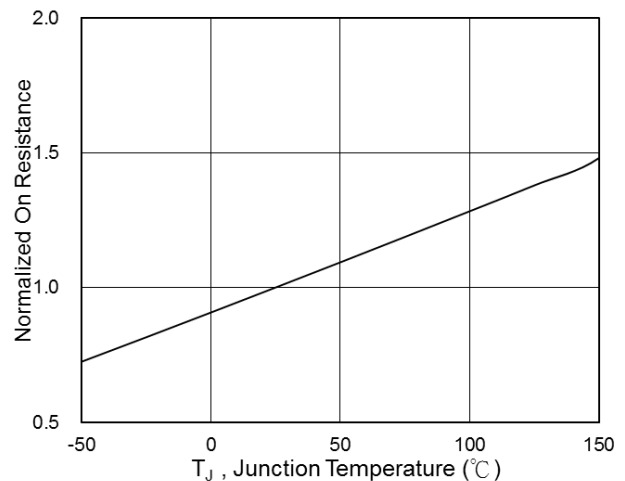


Fig.11 Unclamped Inductive Switching Waveform

P-Channel Typical Characteristics

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage

Fig.3 Source Drain Forward Characteristics

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J

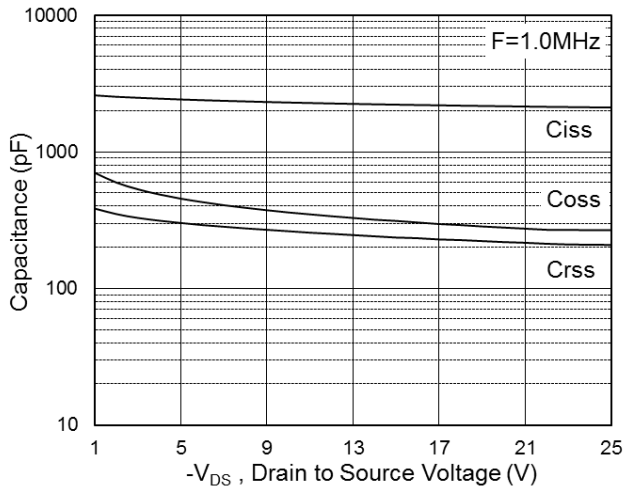


Fig.7 Capacitance

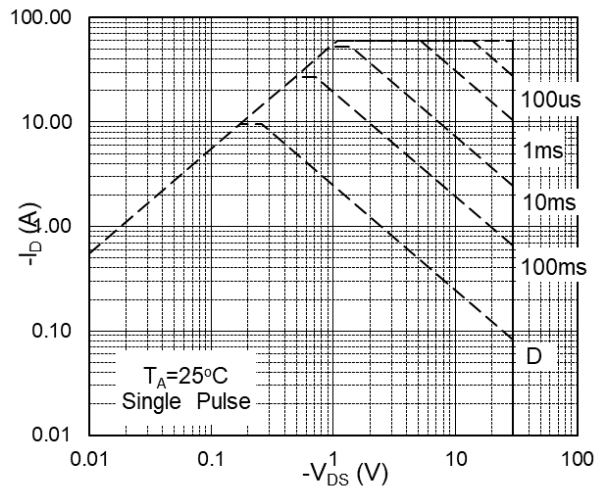


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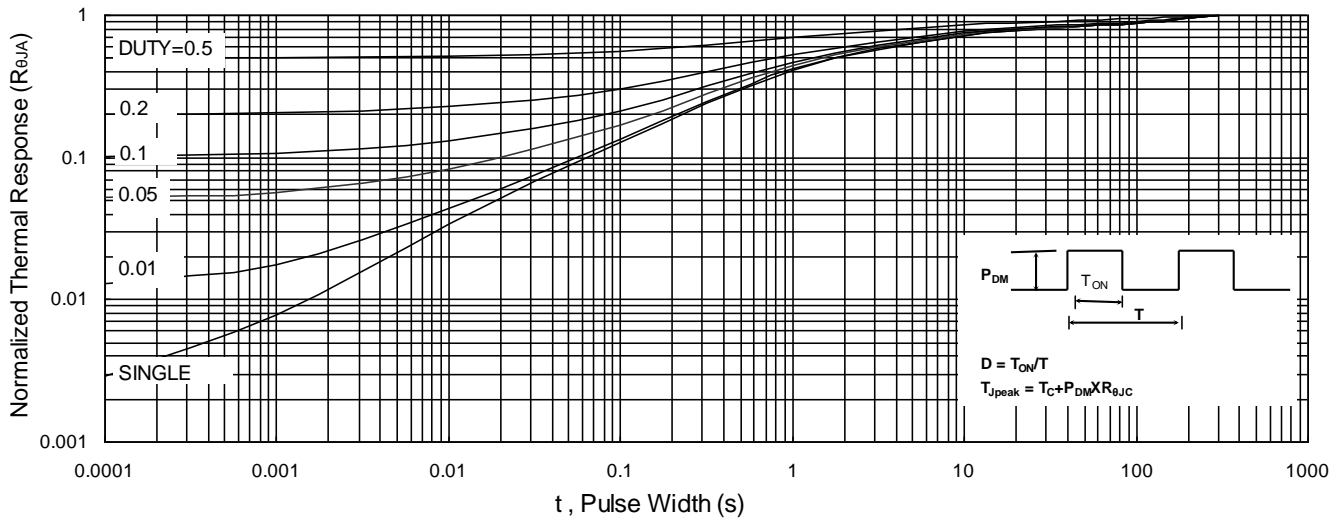


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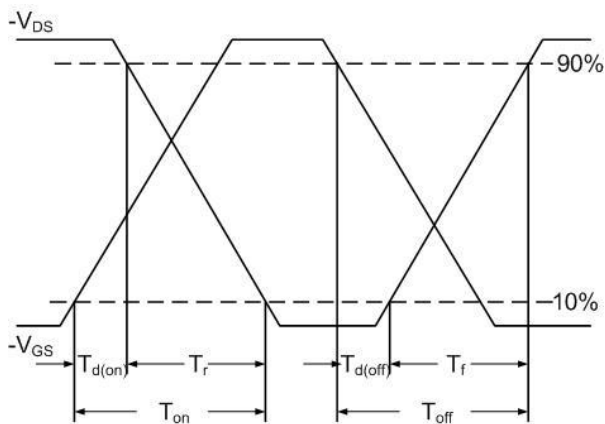


Fig.10 Switching Time Waveform

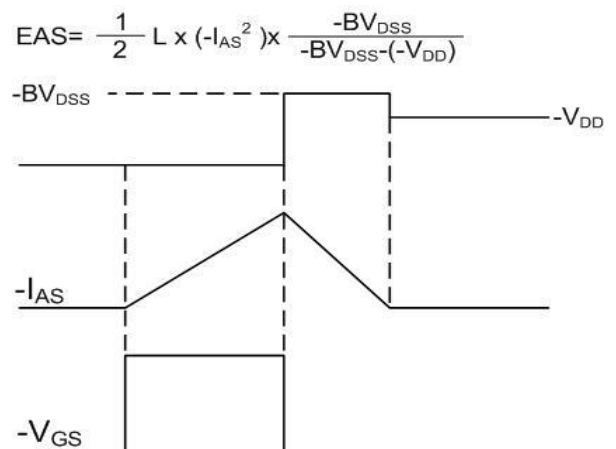
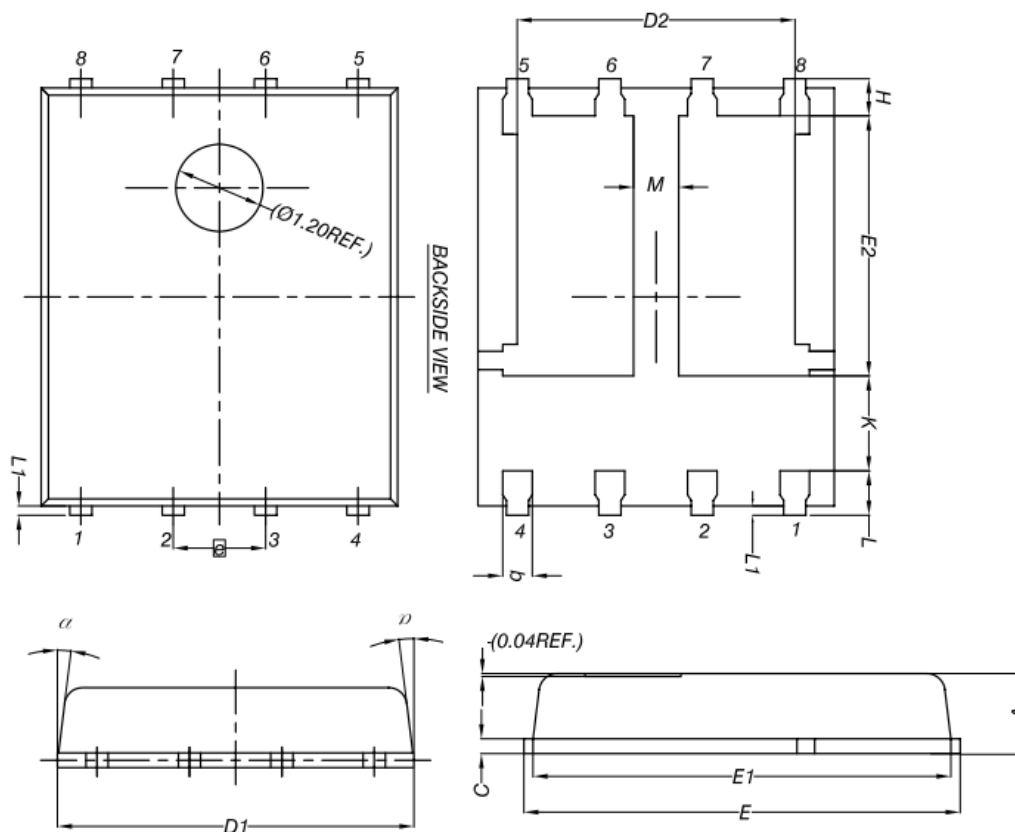


Fig.11 Unclamped Inductive Switching Waveform

PRPAK5X6 Package Outline Dimensions



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
M	0.50	-	-
α	0°	-	12°

